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Ferroelectric Nanogap-Based Steep-Slope Ambipolar Transistor

*Yaodong Guan, Zhe Guo, and Long You**

The subthreshold swing (SS) of metal–oxide-semiconductor field-effect transistors is limited to 60 mV dec^{-1} at room temperature by the Boltzmann tyranny, which restricts the scaling of the supply voltage. A nanogap-based transistor employs a switchable nanoscale air gap as the channel, offering a steep-slope switching process. Meanwhile, nanogaps featuring even sub-3 nm can efficiently block the current flow, exhibiting the potential for tackling the short-channel effect. Here, an electrically switchable ferroelectric nanogap to construct steep-slope transistors, is exploited. An average SS of 15.9 mV dec^{-1} across 5 orders and a minimum SS of 13.23 mV dec^{-1} are obtained in the high current density range. The transistor exhibits excellent performance with near-zero off-state leakage current and a maximum on-state current of 202 µA µm^{-1} at V_{DS} = 0.5 V. In addition, the transistor can turn off with either a positive or negative increase in the gate voltage, exhibiting ambipolar characteristics.

1. Introduction

In the new era of hyper Moore's law, one of the main challenges is supply voltage reduction for dynamic power dissipation. In conventional complementary metal–oxide-semiconductor (CMOS) technologies, the supply voltage has not significantly decreased for nearly a decade, although conventional geometric scaling has been ongoing. This is owing to a fundamental bottleneck in the subthreshold swing (SS), which is defined as the gate voltage variation required to change the drain-to-source current (I_D) by a decade. In the metal–oxide-semiconductor field-effect transistor (MOSFET), the electron density $n(E)$ in the source can be approximated as the Boltzmann distribution ($n(E) \sim \exp[(E_F\text{-}E)/kT]$) with a long thermal tail above the Fermi level E_F, where k and T denote Boltzmann's constant and temperature, respectively.[1,2] The fundamental thermionic emission of carriers limits the SS to be no less than $2.3kT/q$ (or 60 mV dec^{-1} at room temperature), also known as "Boltzmann limitation,"[3,4] where q denotes the elementary charge. Therefore, it is necessary to seek novel device platforms to overcome this limitation and reduce the SS to sub-60 mV dec^{-1}. Fortunately, several steep-slope devices have been proposed to realize an SS of sub-60 mV dec^{-1}, such as tunnel field-effect transistors (TFETs),[1,5,6] Dirac-source field-effect transistors (DSFETs),[2,7,8] negative-capacitance field-effect transistors (NCFETs),[9–12] nano-electromechanical field-effect transistors (NEMFETs),[13–17] and phase-transition field-effect transistors.[18,19] Emerging steep-slope field-effect transistor (FET) technologies with novel principles have been extensively studied.[20] According to the formula for SS, which is given as $(\partial V_G/\partial\Psi_S)[\partial\Psi_S/\partial(\log_{10}I_D)]$ (where V_G, I_D, and Ψ_S are the gate voltage, drain current, and channel surface potential, respectively), the goals of these technologies can be divided into two categories: lowering the transport factor $\partial\Psi_S/\partial(\log_{10}I_D)$ or reducing the body factor $\partial V_G/\partial\Psi_S$.[8] The body factor can also be expressed as $1+C_s/C_{ins}$ (C_s and C_{ins} denote the substrate capacitance and insulator capacitance, respectively), which is usually larger than 1.[1] However, it is noted that an ideal logic transistor prefers to have an ultralow SS value while maintaining a large on-current, in other words, it should switch from the beginning of the subthreshold region. Thus, it is desirable to develop transistors with high steep-sloped current densities.

The representations of the transport factor reduction-induced steep-slope FETs are the TFETs and DSFETs. TFETs utilize quantum mechanical band-to-band tunneling from the valence band to the conduction band instead of thermionic carrier injection in conventional MOSFETs.[1,21,22] The main challenge in TFETs is to realize a high on-state current.[8,23] In DSFETs, a Dirac material with linear energy dispersion near the Dirac point is used as the source material.[2] Therefore, the Dirac source cuts off the long thermal tail and exhibits a more localized electron distribution. This electronic refrigeration effect lowered the transport factor.[8] Nevertheless, ultralow SS could be difficult to implement based on such a mechanism, and the performance of DSFET is strictly related to the quality of Dirac materials, whose preparation and device construction pose some challenges.

The other category includes NCFETs, NEMFETs, and phase-transition FETs in which the body factor can be reduced below

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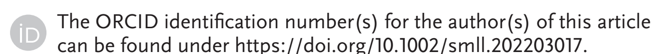
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1.[12,13,18,24,25] To construct transistors, NCFETs introduce ferroelectric materials into the gate dielectric stack. The incorporation of a ferroelectric material triggers internal gate voltage amplification behavior and thus a high Ψ_S, thereby reducing the body factor and achieving sub-60 mV dec^{-1} SS.[25] Phase-transition FETs employ a metal–insulator transition material (such as VO_2) attached to the source terminal while the abrupt transition process tends to occur near the off-state.[18] Similarly, the filament transistors employing the formation and rupture of metallic filaments in the conducting bridge random access memories have achieved record low SS (0.24 mV dec^{-1}). But it faces the challenge that the different drain polarity is needed to change its resistance states.[26] Abrupt switching from the on-state can be easily observed in NEMFETs, which utilize a mechanically movable gate or body through electrostatic force.[13,14,27,28] The NEMFET can accomplish an on–off switch corresponding to a dinky gate voltage change. However, with device scaling down, the precise control of nanogap switching by electrostatic force could become challenging.[29] A relatively high contact resistance may also decrease the on-state current. Moreover, as the core of NEMFETs, a switchable nanogap is usually formed by the final "release" etching step using highly stringent fabrication processes.[29,30]

According to the principle of NEMFETs, the transistor in a mechanical switching manner can, in principle, achieve abrupt switching from the beginning of the subthreshold region. In this study, we use a ferroelectric nanogap (FN) to construct a novel steep-slope transistor. In contrast to NCFETs, the ferroelectric material involved in our configuration is aimed at producing the switchable nanogap by the ferroelectric domain switching-induced strain in a local region. As the nanogap opens and closes in mechanically, ultralow SS and high steep-slope current densities are obtained. An inverter logic based on an FN transistor (FNT) has also been demonstrated. Furthermore, because ferroelectric domain switching is dominated by the applied electric fields, a sub-1 V operating voltage is expected by reducing the ferroelectric material thickness. Our study reveals that the FNT has the potential to be a new type of emerging steep-slope device for beyond-CMOS technologies.

2. Results and Discussion

2.1. Device Structure and Nanogap Morphology

Under the action of an electric field, the ferroelectric domains in a ferroelectric single crystal undergo specific switching. The switching-induced elastic energy could cause the appearance of a nanogap along the domain boundary, as discussed in our previous works.[31,32] If there is a metallic thin film on top of the ferroelectric material, a nanogap is also created in the film when it propagates through the film. Therefore, it is possible to use a simple method to prepare extremely small air nanogaps without involving complicated fabrication processes, as in traditional nanoelectromechanical switches.[33] **Figure 1**a

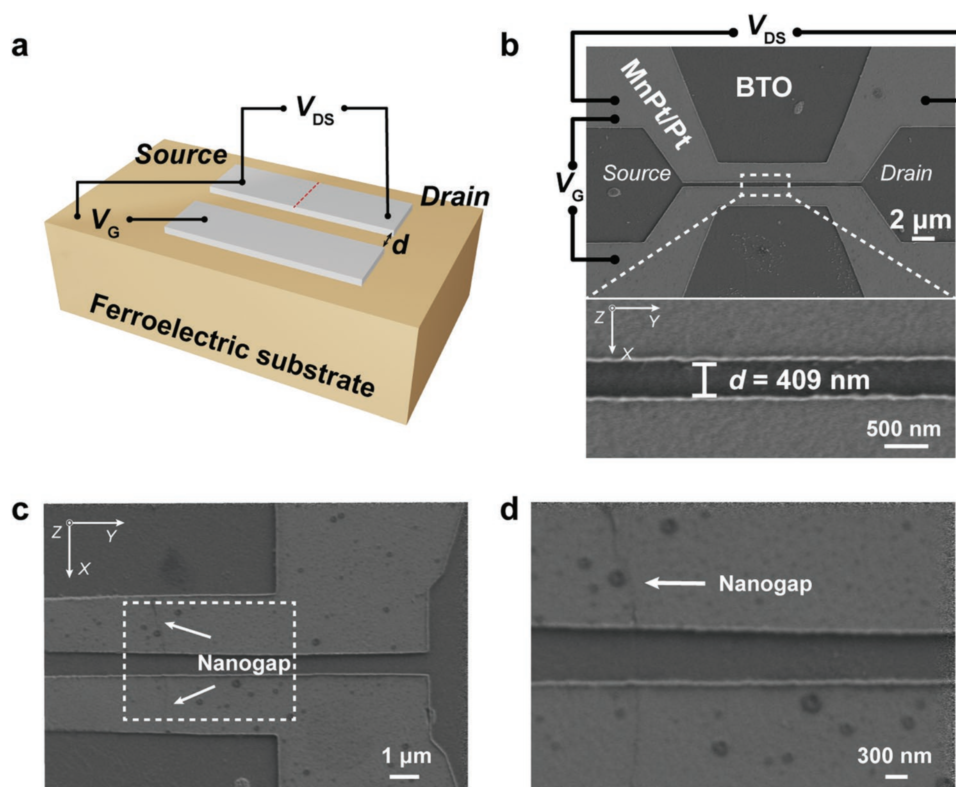

Figure 1. FN transistor and Ferroelectric nanogap. a) Schematic of FN transistor and measurement setup. b) Top-view SEM image of one fabricated device with the parallel strips for electrical measurement. Scale bar: 2 µm. The bottom panel shows an enlarged view of the parallel strips. Scale bar: 500 nm. c) Morphology of induced FN at $V_G = 0$ V. Scale bar: 1 µm. d) Enlarged view of white dashed-line rectangle in (c). Scale bar: 300 nm. The V_G pulse for nanogap forming is ±40 V.

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shows a schematic of the ferroelectric nanogap transistor and the measurement setup. The metallic thin films were patterned into parallel strips to apply a voltage (V_G) to trigger ferroelectric domain switching. In the actual experiments, we used a (100)-oriented $BaTiO_3$ (BTO) single crystal as the ferroelectric substrate with a thickness of 500 µm, which is a tetragonal (*T*) phase at room temperature. The $Mn_{50}Pt_{50}$ (MnPt, 40 nm)/Pt (5 nm) bilayer films were deposited on the substrate by sputtering at room temperature. MnPt has moderate mechanical performance and possesses a balance between ductility and brittleness;[34] therefore, the nanogap in the film can be easily switched between the open and closed states. The top Pt layer increased the channel conductivity in the closed state of the nanogap. Figure 1b illustrates the top-view SEM image of one fabricated device for electrical measurements with a distance (*d*) of ≈400 nm between the parallel strips. Notably, a high electric field can be acquired by simply decreasing this distance, which will be discussed later. After completing device fabrication, the nanogap forming process was performed by repeatedly applying an alternating V_G pulse until the nanogap was induced. The detailed formation process has been described previously.[32] The SEM image in Figure 1c illustrates the morphology of induced ferroelectric nanogap, which was captured from a similar device at $V_G = 0$ V (corresponding to the closed state). A shallow trace along the *x*-direction was visible, as indicated by the white dashed-line rectangle, and an enlarged view is shown in Figure 1d.

2.2. Transfer Characteristics and Mechanism of Ambipolar Switching

Figure 2a shows the room-temperature transfer characteristics (I_D–V_G) of the FNT at $V_{DS} = 50$ mV (see the linear-scale curve in Figure S1, Supporting Information). At $V_G = 0$ V, the nanogap is closed, and accordingly, current can flow between the source and drain when V_{DS} is applied. As V_G increased monotonically up to the threshold voltage (V_T), abrupt switching from the on-state was observed, and a high on/off current ratio (≈10^6) at $V_{DS} = 50$ mV was achieved, indicating the opening of the nanogap. Once V_G is scanned back from −36 V to the vicinity of V_T, abrupt switching from the off to on state occurs. The forward and backward sweeping loops demonstrate a small hysteresis. This behavior is similar to that of an n-channel depletion-mode MOSFET. Intriguingly, with a positively increased V_G, the transistor turned off again, similar to the p-channel mode, as shown in Figure 2b. Thus, our transistor exhibits ambipolar characteristics.

Next, we discuss the possible underlying mechanism of ambipolar switching. *T*-phase ferroelectric oxides usually have

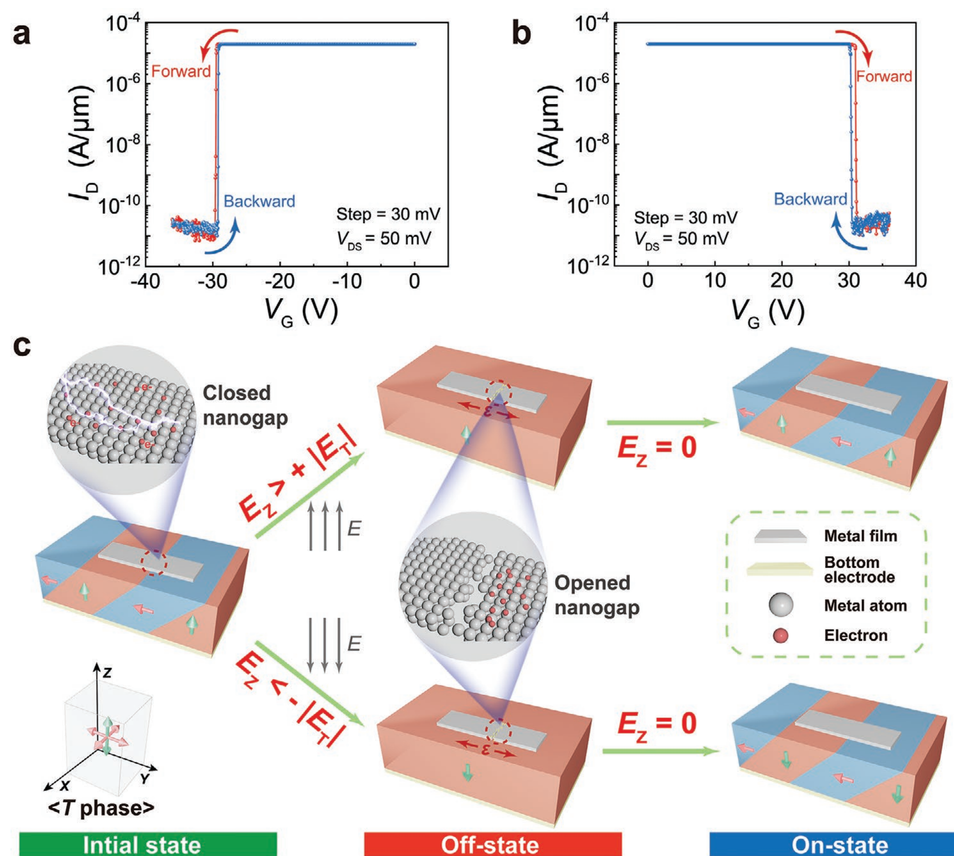

Figure 2. Transfer characteristics and mechanism of ambipolar switching. a,b) Transfer characteristics (I_D–V_G) of FN transistors with n- and p-type at $V_{DS} = 50$ mV, respectively. V_G step is 30 mV. c) The schematics and working principle of FN transistor. The reversible ambipolar switching of the transistor is demonstrated. The schematic of the metal atomic layer visualizes the state of the current path.

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six spontaneous polarization directions (Figure 2c), which can be divided into two types of domains: out-of-plane domains (i.e., *c* domain, red parts) and in-plane domains (i.e., *a* domain, blue parts). As discussed in our previous work, in the configuration shown in Figure 1a, the *z*-components of the electric fields (E_z) underneath the metallic thin film produced by V_G are much larger than the *x* and *y* components and thus play a key role in the domain switching. With a positive increase in E_z to the threshold E_T, the *a* domains switch to *c* domains. Correspondingly, an in-plane tensile strain (ε) is produced in the domain boundary (see detailed discussions in Note S1, Supporting Information). Consequently, the nanogap in the film is driven open. The source and drain were blocked by air such that no current can flow between them, corresponding to the off-state of the transistor. At this point, E_z is sufficiently high to stabilize the monodomain state (or unstable state). Then, once the gate voltage (or E_z) decreases to the vicinity of the threshold, it is preferred to form the multidomain state again from the energy view. According to previous studies,[35–37] the domain texture could return to the same structure as the previous texture owing to pinned sites such as nanoscale defects. Thus, small hysteretic switching, even hysteresis-free switching, can be obtained. Similarly, with a negative increase in E_z, all domains switch to the *z*-direction (green parts), causing in-plane tensile strain again. Hence, ambipolar switching characteristics were acquired in our FNT.

In our previous studies,[31–33] it is noted that the nonvolatile transfer curves with large hysteresis are observed. A (001) $0.7PbMg_{1/3}Nb_{2/3}O_3$-$0.3PbTiO_3$ (PMN-PT) single crystal, which has a rhombohedral phase at room temperature, was used as the ferroelectric substrate in these studies. The nonvolatile strain produced by 109° domain switching causes a nonvolatile transfer curve, which is significantly different from our results. These results indicate that the switching characteristics of ferroelectric nanogap-based devices are strictly determined by the domain switching process, which also offers routes for designing other functional devices with ferroelectric nanogaps.

2.3. Small SS Value and Large On-Current

Figure 3a,b shows the local enlarged view of the transfer characteristic curves of the n-type (Figure 2a) and p-type (Figure 2b) transistors, respectively. Figure 3c,d illustrates the extracted SS–I_D characteristics of the two types of transistors from Figures 3a, and 3b, respectively. An ultralow minimum SS (SS_{min}) of 13.23 mV dec^{-1} was achieved during the backward sweep of the n-type device. In addition, from the subthreshold region of the n-type FNT (Figure 3a), the average SS ($SS_{average}$) in the backward sweep is 15.9 mV dec^{-1}, which has a large I_D range (across five decades). These results clearly reveal that the FNT scheme can effectively decrease the SS to sub-60 mV dec^{-1}. The mechanical switching method was considered to enable significantly reduced SS values. To demonstrate the good performance of our FNT, we compared it with other representative steep-slope transistors in our study. For instance, the TFET has an $SS_{average}$ of 31.1 mV dec^{-1} across 4 decades,[1] the NCFET presents an $SS_{average}$ of larger than 41.7 mV dec^{-1} across 5 decades,[11] and the DS-FET exhibits an $SS_{average}$ of 35 mV dec^{-1} across 3 decades.[7] Clearly, our FNT has the smallest $SS_{average}$ compared with the aforementioned transistors. More recently, a record low $SS_{average}$ (0.24 mV dec^{-1}) over 5 decades has been reported in the filament transistor which exploits conductive bridge random access memory (CBRAM) attached to the source terminal of a conventional metal–oxide-semiconductor transistor.[26] But different drain polarity is

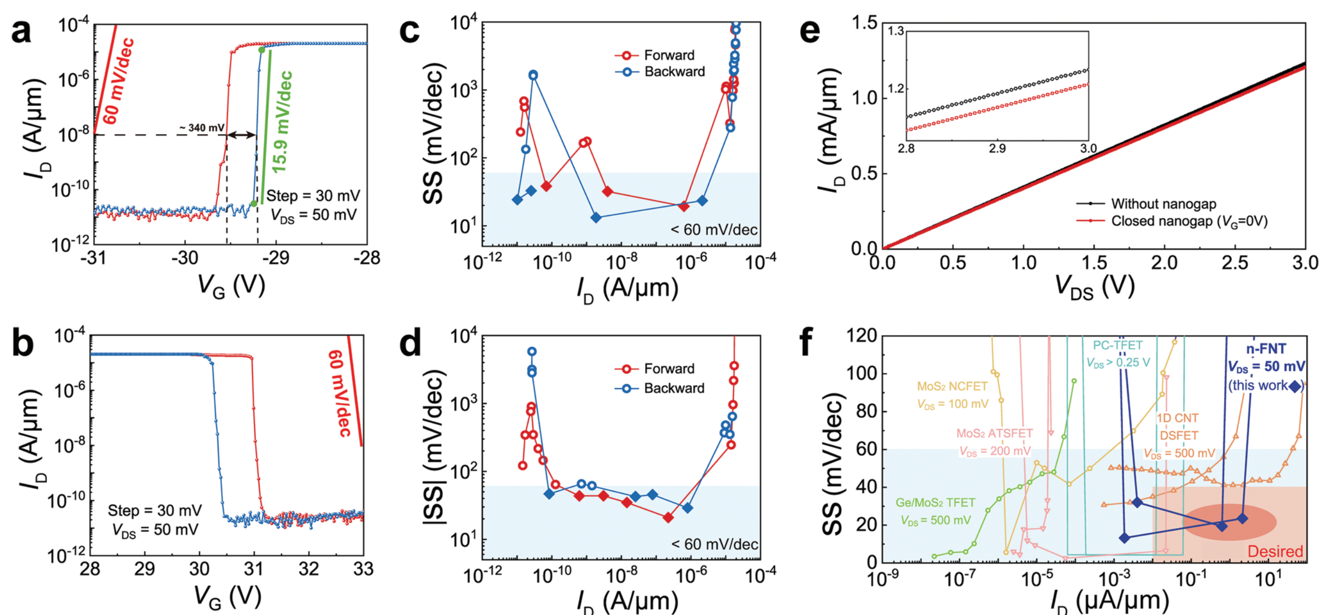

Figure 3. a,b) Local enlarged view of the transfer characteristic of n-type (Figure 2a) and p-type (Figure 2b) transistors, respectively. Average SS of 15.9 mV dec^{-1} over 5 orders in n-type device is displayed. c,d) Extracting SS as a function of I_D from (a) and (b), a minimum SS of 13.23 mV dec^{-1} is achieved in the reverse sweep of n-type device. e) I_D as a function of V_{DS} and the transistor is characterized for ohmic behavior when the nanogap is closed. f) Our FNT with other state-of-the-art steep-slope transistors, including TFET,[1] 1D DSFET,[7] NCFET,[11] PC-TFET,[39] and 2D ATSFET.[40] Our FN transistor possesses higher steep-slope current densities even at V_{DS} = 50 mV.

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needed to change its resistance states. On the other hand, in our FNT, the smallest hysteresis is observed at ≈340 mV, as shown in Figure 3a.

One of the main concerns is the contact resistance of the closed state of the nanogap, which determines the on-state currents. We measured I_D as a function of V_{DS}, and the results are shown in Figure 3e. A linear relationship between I_D and V_{DS} was observed, indicating an ohmic contact. Compared to the I_D–V_{DS} curve of the device without a nanogap (the black line in Figure 3e), the negligible difference indicates that the source and drain electrodes were in close contact in the on-state, which was unaffected by the occurrence of the nanogap. Therefore, the on-state resistance of the transistor was determined by the conductivity of the metallic thin films. As expected, high on-currents of 202 and 1208 μA μm^{-1} were obtained at V_{DS} = 0.5 and 3 V, respectively. We measured the transfer curves under different drain biases (Figure S2, Supporting Information), and the proportional relationship between the on-current and drain biases again proved the ohmic contact across the nanogap. We also measured the off-state current as a function of V_{DS} (Figure S3, Supporting Information), which has several picoampere orders and can be attributed to measurement noise.[38] Our transistor also exhibited good stability under voltage pulse tests (Figure S4, Supporting Information). In addition, our FNT exhibited a relatively wide working temperature range from 200 to 410 K (Figure S5, Supporting Information).

It is ideal for transistors to have a small SS value while maintaining a large on-current, which is a key metric for logic transistors to benefit from steep slopes.[8] The SS as a function of I_D was compared with other state-of-the-art steep-slope transistors, including TFET,[1] 1D DSFET,[7] NCFET,[11] hybrid phase-change-tunnel FET (PC-TFET),[39] and 2D atomic threshold switching (ATSFET),[40] as shown in Figure 3f. Our FNT possesses superior steep-slope current densities compared with other technologies. Note that the current density was obtained at V_{DS} = 50 mV, and higher values can be expected at a larger V_{DS}.

2.4. Implementation of Inverter

Then, we demonstrate inverter logic based on the FNT. **Figure 4**a illustrates the circuit diagram of one transistor-only inverter with a pull-down load. The input signal V_{in} is the potential difference between the two parallel electrodes in the device, which is defined as $V_{gap} - V_{side}$ (Figure 4a). V_{gap} refers to the potential of the electrode where the nanogap is located and V_{side} refers to the potential of the other electrode. An R_0 of 1 MΩ was used as a voltage divider resistor, and an R_1 of 47 kΩ was the current-limiting protection resistor. When a small V_{in} (less than the switching voltage) is applied, the nanogap is closed and the transistor is in the on-state. The output voltage V_{out} is equal to the divided voltage of resistor R_0, which is approximately equal to the entire V_{DD}. When V_{in} is greater than the switching voltage, the nanogap opens and the transistor turns off. The output voltage is ≈0. Figure 4b shows the output characteristics of the inverter and corresponding gain values at V_{DD} = 5 V. The highest gain of 17.68 was achieved.

2.5. Top-Gate Structure Design

For large-scale applications, the top-gate configuration used in conventional MOSFET is preferred. The top-gate design comprising the core structure is shown schematically in **Figure 5**a. In such a structure, a ferroelectric oxide film is employed, sandwiched between the top-gate electrode and the bottom conductive layer. The perpendicularly applied V_{GS} was responsible for the switching of the nanogap, and V_{DS} was used to detect the resistance states. To optimize the structure, a buffer layer underneath the conductive electrodes, into which the nanogap can easily extend, is inserted between the substrate and the conductive source, and drain layers. In recent years, BTO thin films have been fabricated on silicon substrates, which is beneficial for compatibility with the CMOS technology.[41–43] Moreover, the HfO_2-based thin films, which exhibit ferroelectric characteristics and are compatible with silicon technology, could also be applied to our technology.[44,45]

We note that a high operating voltage is demonstrated in our transistor, which is mainly owing to the high thickness of the bulk BTO substrate. Because the switching mechanism of the FNT originates from electric-field-induced ferroelectric domain switching, the operating voltages can be reduced by reducing the thickness of the ferroelectric layer. Thus, a low operating voltage was expected in the top-gate structure. Here, we exploit the COMSOL simulations to estimate the operating voltage

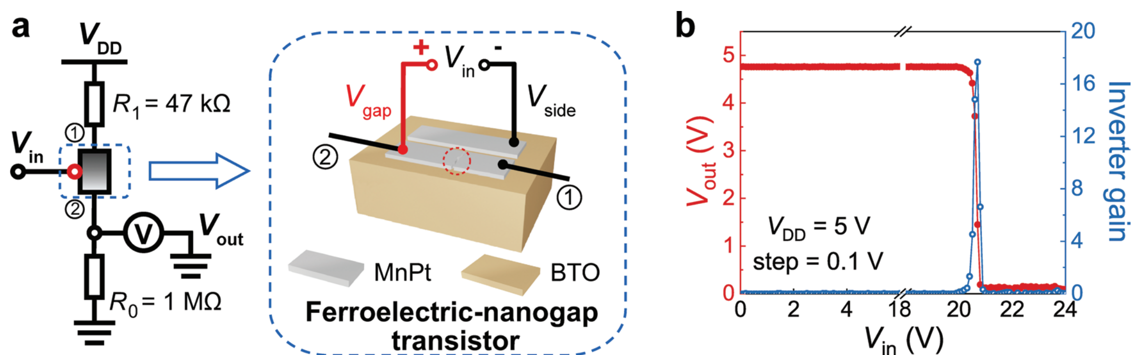

Figure 4. Implementation of inverter. a) Circuit diagram of one transistor-only inverter with a pull-down load. b) Output characteristics of inverter and corresponding gain values.

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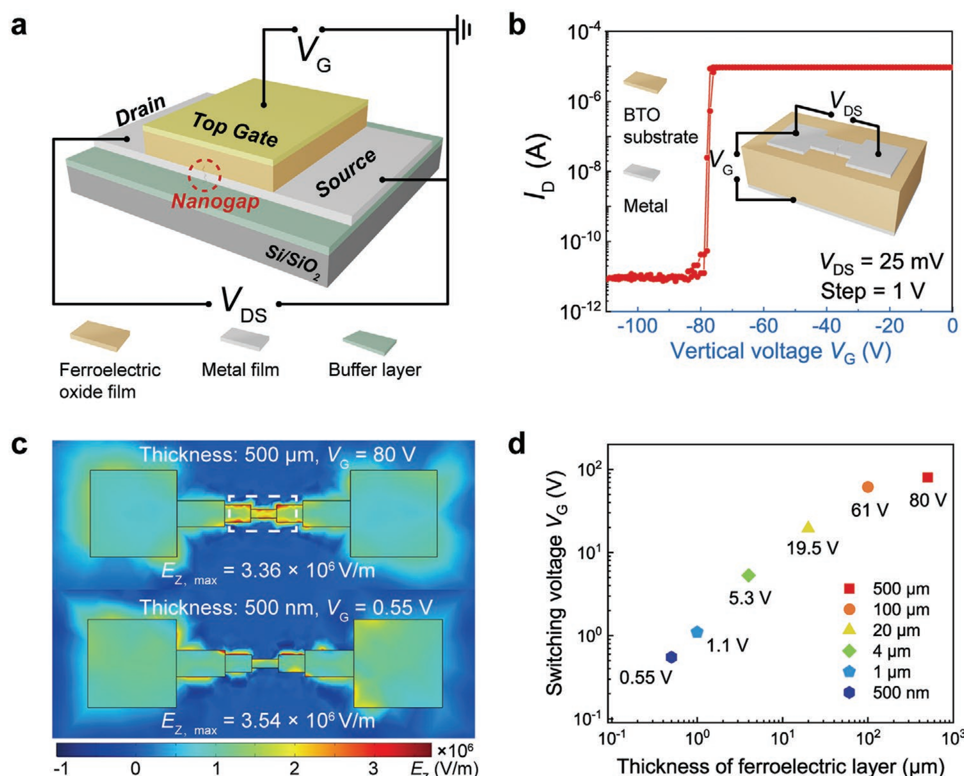

Figure 5. Top-gate structure design. a) Schematic diagrams of top-gate configuration FN transistor. b) The I_D–V_G transfer characteristics of a back-gate structure device. The switching voltage of this FN transistor is ≈80 V. The V_G pulse for nanogap forming is ±170 V. Inset: the structure of back-gate FN transistor. c) *z*-components of electric field simulated by COMSOL software for 500 μm and 500 nm thickness of ferroelectric layer at V_G = 80 and 0.55 V, respectively. The maximum value of E_Z is similar in both cases. d) Switching voltages for devices with different thicknesses of ferroelectric layer.

based on experimental results from a back-gate device using the BTO bulk substrate. The I_D–V_G transfer characteristics of a back-gate device are shown in Figure 5b, where the thickness of BTO substrate is 500 μm. At the switching voltage (≈80 V), the electric field distributions were obtained via simulations (top panel of Figure 5c). In the central area of the device (white dashed line), the maximum E_z reached 3.36 × 10⁶ V m⁻¹. For ferroelectric layers of different thicknesses, we can achieve the same or similar electric field distributions by adjusting the applied V_G. For instance, when the thickness of the ferroelectric layer decreases to 500 nm, V_G of 0.55 V can trigger a similar electric field distribution with maximum E_z reaching 3.54 × 10⁶ V m⁻¹, as shown in the bottom panel of Figure 5c. Then, we extracted V_G as the switching voltage for this thickness (500 nm). As shown in Figure 5d, as the thickness decreases, the switching voltages shrink quickly and sub-1 V operation can be potentially achieved when the thickness of the ferroelectric layer is 500 nm. More recently, a study experimentally demonstrated a low switching voltage (<100 mV) for BTO thin films with thicknesses less than 150 nm,[46] which facilitates our nanogap-based transistor to have a low gate voltage.

3. Conclusion

In conclusion, a new steep-slope ambipolar transistor based on a switchable nanogap is demonstrated, which exhibits an average SS of 15.9 mV dec⁻¹ and minimum SS of 13.23 mV dec⁻¹. Owing to the metallic ohmic contacts between the source and drain, a high on-state current of 202 μA μm⁻¹ at V_{DS} = 0.5 V was achieved. In addition, the existence of an air nanogap enables a negligible off-state leakage current, which allows low static power consumption. By further reducing the dimensions of device, a sub-1 V operation can be obtained. These results demonstrate the potential for developing an excellent steep-slope transistor beyond-CMOS technology. However, there are still numerous further optimization studies that require the joint efforts of researchers, such as more stable free hysteresis and electrodes resistant to oxidation and fracture. Ferroelectric domain engineering, hermetic packaging, and alternative electrode materials are potential solutions for these issues.

4. Experimental Section

Sample Growth: A 5 × 5 μm² area, 500 μm thick (100)-oriented $BaTiO_3$ single crystal was used as the ferroelectric substrate. 40 nm thick layer of MnPt was sputtered from MnPt target on the $BaTiO_3$ substrate by radio frequency (RF) sputtering system with a base pressure of 1.5 × 10⁻⁵ Pa at room temperature (RF power of 20 W, argon (Ar) gas pressure of 0.2 Pa, and Ar at 20 sccm flow). The sputtering time was 12 min. Then, a 5 nm thick layer of platinum (Pt) was deposited on top of the MnPt using direct current sputtering.

Device Fabrication: The device patterns with nanoscale were defined using standard e-beam lithography (EBL) process followed by argon ion beam etching to sputter-etch the MnPt and Pt layers. The back-gate electrodes of the FNT were defined by lithography and argon ion beam

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etching. In back-gate device, the $BaTiO_3$ substrates were coated silver (Ag) on the backside for bottom conductive layer.

Electrical Measurements: The electrical contacts on the MnPt/Pt film were made of aluminum (Al) wires by wire bonding. The V_G pulse for nanogap forming was applied by Keithley 2400. The transfer characteristic measurements of the FNTs with the parallel strips were performed by semiconductor parameter analyzer (Keysight B1500A) in an ambient atmosphere at room temperature. These were done by sweeping the voltage from 0 to 36 V (or −36 V) in steps of 30 mV. The transfer characteristic measurement of the back-gate transistors was performed by Keithley 2400 and 2450 in a vacuum chamber of 6×10^{-5} mbar at room temperature. This was done by sweeping the voltage from 0 to −110 V in steps of 1 V. The electrical performance of inverter was measured by the combination of Keithley 2400, 2450, and 2182 A. Devices were placed in a closed chamber in a vacuum chamber of 6×10^{-5} mbar for the switching performance tests under different temperatures. The temperature was controlled by balancing the heating wire with liquid nitrogen. The repeatability test was performed in a vacuum chamber of 6×10^{-5} mbar.

Morphological Characterization: The morphology of the FNT was characterized by SEM imaging (Zeiss GeminiSEM 300-71-12). The top-view SEM image of one FNT was obtained using a magnification of ×3.5 k, an acceleration voltage of 3.0 kV, and a working distance of 6.4 mm. The enlarge-view image of above device was obtained using a magnification of ×15.0 k, an acceleration voltage of 3.0 kV, and a working distance of 6.4 mm. The SEM image of induced ferroelectric nanogap was obtained using a magnification of ×7.92 k, an acceleration voltage of 2.0 kV, and a working distance of 8.1 mm. And the enlarge-view image of nanogap was obtained using a magnification of ×19.56 k, an acceleration voltage of 2.0 kV, and a working distance of 8.1 mm. The SEM images were a bit blurry due to the super insulating properties of the $BaTiO_3$ substrates.

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

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Conflict of Interest

The authors declare no conflict of interest.

Author Contributions

Y.G. and Z.G. contributed equally to this work. L.Y. and Z.G. conceived the idea. Z.G. deposited the film. Y.G. fabricated the devices. Y.G. and Z.G. performed the electrical measurements and analyzed the results. Y.G. conducted the SEM characterizations. Y.G, Z.G., and L.Y. wrote the manuscript. All authors commented on the manuscript.

Data Availability Statement

The data that support the findings of this study are available from the corresponding author upon reasonable request.

Keywords

beyond complementary metal–oxide-semiconductors, ferroelectric nanogaps, ferroelectronics, negligible off-current, steep-slope transistors

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