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Low-energy complementary ferroelectric-nanocrack logic

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ABSTRACT

Ferroelectric-based electronic devices have excellent low-energy characteristics due to the highly insulating property, in which the Joule heating can be neglected. The recent discovery of electrically switchable cracks in ferroelectric/alloy film heterostructure gave rise to a new way to construct transistor, where the opening and closing of crack switched the channel current off and on. Here, we observed the complementary switching of cracks for the first time, and demonstrated a complementary inverter without any additional process to set different types of transistors, which was implemented by forming the n- and p-type transistor in conventional complementary metal oxide semiconductor (CMOS) technology. The complementary states were generated spontaneously once the cracks were induced and varied with the change of applied input voltage polarity. The low ON resistance and near-zero OFF state leakage current result in the high current on/off ratio ($\sim 10^7$) and allow for the low dynamic and static power dissipation. Further, the switching of cracks is coupled to the surrounding ferroelectric polarization states, offering the non-destructive readout operation. We believe that our work provides a very simple route to build complementary logic gates and paves a way for the energy-efficient electronic devices, while promoting the "crack nanoelectronics".

1. Introduction

Ferroelectric-based electronic devices code the digital memory or logic states through switching the polarization directions by the external electric fields/voltage, and usually feature the non-volatility, fast switching speed and almost unlimited endurance cycles [1–3]. Typically, the intrinsic highly insulating property enables the ultralow leakage current, which exactly meets the quest for the low power consumption. However, the conventional ferroelectric-capacitor device is limited to its destructive readout process, which requires a rewrite operation [4]. The ferroelectric tunnel junction based devices, which can detect the polarization states nondestructively, face the difficulty for fabricating the ultrathin ferroelectric film with high quality [5]. Recently, the emerging charged domain walls based devices associate the polarization states with the conductance of the domain wall [6–9]. Such the device offers the possibility for ultra-high density integration as the domain size can be as small as several nanometers, but the low conduction current is insufficient to drive the high speed read-out operation, which is particularly crucial for the logic computing. In addition, the ferroelectric field effect transistor (FET) or the negative capacitance FET, which contain a ferroelectric oxide in the gate insulator, can attain a lower subthreshold swing voltage than the Boltzman limit (60 mv/dec) and thereby enable a low power operation [10,11]. But the static leakage currents still exist in such the FET, whereas the near-zero standby power is highly desirable.

The mechanical switch can thoroughly break the current path relying on the formed air gap, offering intriguing possibilities for the ultralow power consumption. Such the switching has also been discovered in the ferroelectric-based devices. Very recently, in the ferroelectric/metal alloy film heterostructure, based on the electrically switchable crack

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with nanoscale width, an energy-efficient device for the memory application has been demonstrated [12,13]. As schematically shown in Fig. 1a, this crack extending from the ferroelectric oxide into the alloy film, forms an air gap between electrodes during it is open (see the cross-sectional images in reference 12). On the contrary, when the crack is closed, the current flows smoothly due to the close metal contacts. Importantly, the opening and closing of the crack are considered as originating from the domain switching, offering a non-destructive readout operation of polarization states.

On the other hand, the complementary logic gates possess exceptional low power characteristics, in which either the constituent n-type or p-type transistor is always at the OFF state, and has greatly promoted the development of modern microelectronics in the last forty years. However, in the current silicon-, carbon nanotube- or two-dimensional materials-based complementary logic, the physically, chemically doping process or the additional gate electrode is required to set the polarity of transistors [14–16]. The complicated doping process irreversibly defines the types of transistor and becomes hard to control with the further miniaturization. And the additional gate could lead to the sophisticated circuit design. Here, the interesting complementary switching of cracks has been investigated for the first time, in which the opening of one crack is accompanied by the closing of the other crack, and fortunately, any effort is not needed to fabricate different types of transistors. As the most representative logic, the NOT-logic based on the ferroelectric-nanocrack has been demonstrated. Moreover, the phase-field simulation is used to explain the switching process of cracks. We believe that this work is a step forward towards the ferroelectric-based logic device with non-destructive readout process and low power consumption.

2. Results and discussion

2.1. Crack evolution induced by ferroelectric domain switching

Here, the single crystal (001)-oriented $0.7PbMg_{1/3}Nb_{2/3}O_3$-$0.3PbTiO_3$ (PMN-PT) and $Mn_{50}Pt_{50}$ (MnPt) were chosen as the ferroelectric oxide and alloy thin film, respectively. Due to the moderate mechanical properties, MnPt thin film is appropriate for generating the switchable cracks [13]. Firstly, the correlation between the crack topography and domain switching, under the in-plane polarization voltage, was studied. As represented in Fig. 1b, the MnPt film is connected to the ground and the piezoresponse force microscopy (PFM) tip is used to apply the polarization voltage. The yellow square (3.5 μm × 3.5 μm) on the PMN-PT surface indicates the polarization area, in which the crack extension from the MnPt film locates. At the initial (Fig. 1cI), the topography image showed that the crack was at the open state, and distinctly two different domains were located at each side of the crack as indicated by the lateral PFM (LPFM) image (Fig. 1cVII). The application of +10 V made no change on the crack and domain states (Fig. 1cII and **1**cVIII). Interestingly, after the application of - 5 V (Fig. 1cIII, **1**cIX and the vertical PFM image in Supplementary Fig. S1), the polarization switching has occurred but the crack remained open, showing a nonvolatile control. However, the increased negative bias voltage (Fig. 1cIV and **1**cX) switched the crack into the closed state and meanwhile transformed the domain into a uniform state on both sides of the crack. On the contrary, the positive bias voltage resulted in the opening of the crack again and the symmetrical evolution process of the domain switching. Clearly, the crack state is strongly related to the domain switching that is determined by the applied electric field; the positive voltage induces the opening of the crack while the negative one corresponds to the closed crack. This phenomenon inspires us to further explore the complementary switching of cracks.

2.2. Complementary switching of cracks

As the schematic shown in Fig. 2a, the deposited alloy thin film is etched into two separated areas and the complementary switching occurs when an in-plane voltage is applied between these two areas. The positive voltage can induce the opening of crack 1 and the closing of crack 2, while the negative voltage exactly reverses the states of cracks (see Supplementary Fig. S2). Fig. 2b shows the fabricated device with a 6 μm gap width between the separated MnPt film areas. Fig. 2c and d show the optical images of the device after applying +20 V and – 20 V gate voltages, respectively. Clearly, under the application of either the positive or the negative voltage, it is always that one crack is distinctly observed and the other one is nearly vanished, presenting the opposite states. The high-resolution scanning electron microscopy (SEM) images (insets in Fig. 2c and d) indicate that the width of the crack is about 30

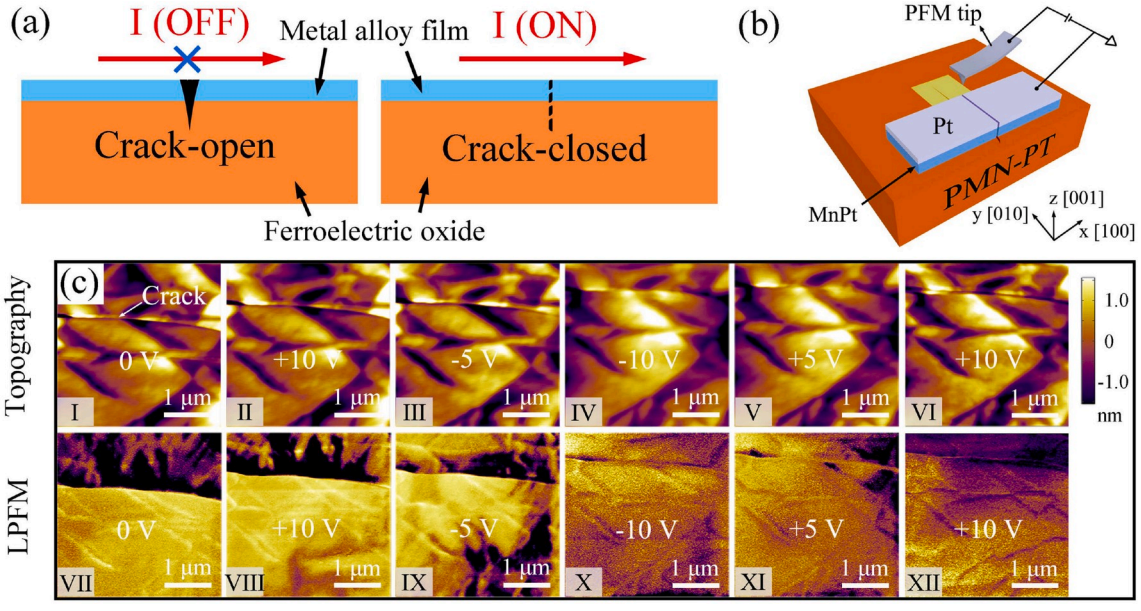

Fig. 1. Ferroelectric domain switching induced crack evolution. **(a)** Schematic of the structure of the crack-based device and the operating principle. **(b)** Schematic of the PFM measurement. The yellow square represents the tip polarization area. **(c)** Topography (I-VI) and LPFM (VII-XII) images of the tip polarization area (3.5 μm × 3.5 μm) under different polarization voltages which range from 0V → +10V→-10V→ +10V.

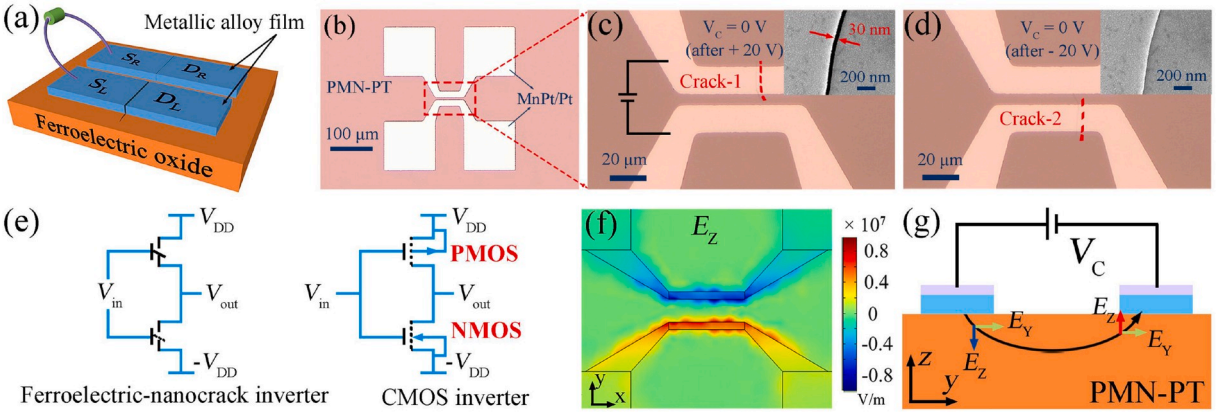

Fig. 2. Schematic and demonstration of the complementary switching of cracks. (**a**) Schematic of the complementary switching of cracks based on the ferroelectric/metallic alloy film heterostructure. (**b**) Optical image of the fabricated device based on the PMN-PT/MnPt heterostructure. (**c**) Optical image of the states of cracks after applying + 20 V between the two separated MnPt film areas. Inset shows the SEM image of partial crack-1, which is at the open state. The red dashed line indicates the crack orientation. (**d**) Optical image of the states of cracks after applying - 20 V. SEM image in the inset shows closed state of partial crack-1, which is the same location as the one in (**c**). (**e**) Complementary ferroelectric-nanocrack inveter and conventional CMOS inverter. (**f**) *z*-component of the electric field in the device shows the opposite directions in the two separated areas. The simulation model has the same gap width as the experimental one and applied V_C is 10V. (**g**) Schematic of the decomposition of the electric fields, which clearly shows that E_z are opposite and E_y are always the same at the symmetrical location.

nm when it is open and the closed crack has a reliable contact. Such the complementary switching is analogous to the CMOS inverter (Fig. 2e), in which one transistor is ON and the other one is OFF. But our crack-based device exploits a very different mechanism to control the channel current and has the ability to break through the physical limitations of conventional transistor [12]. For exploring the reason of the complementary property, we have simulated the electric field distributions using the COMSOL software. Intriguingly, under the applied in-plane voltage, we observed that the *z*-components of electric fields (E_z) had the identical magnitude but opposite directions at the symmetrical locations with respect to the horizontal direction (Fig. 2f). On the contrary, within the MnPt film area, the *y*-components were the same and the *x*-components were so small to be negligible (see Supplementary Fig. S3). This distribution can be easily understood by the decomposition of the electric fields as shown in Fig. 2g. Thus, the complementary switching is mainly attributed to the E_z distribution. So, in our device, the realization of complementary characteristic only depends on the established electric field distribution that is related to the device geometry design.

Next the electrical performance is investigated and the measurement setup is shown in Fig. 3a. V_C is applied to change the states of cracks and a small read signal with a magnitude of 5 mV is used to detect the specific state of each crack. Firstly, the cracks were induced through applying the cyclic V_C with a triangular waveform as illustrated in Fig. 3b (see details in the experimental section). Then the V_C-dependent sweeping loops of the channel current I_1 and I_2 were measured at the same time. As shown in Fig. 3c, I_1 switched from high to low values abruptly with the negative V_C increasing (represented by arrow 1), indicating the crack-1 transformed from the closed to the open state. On the contrary, the similar voltages resulted in the crack-2 changing from

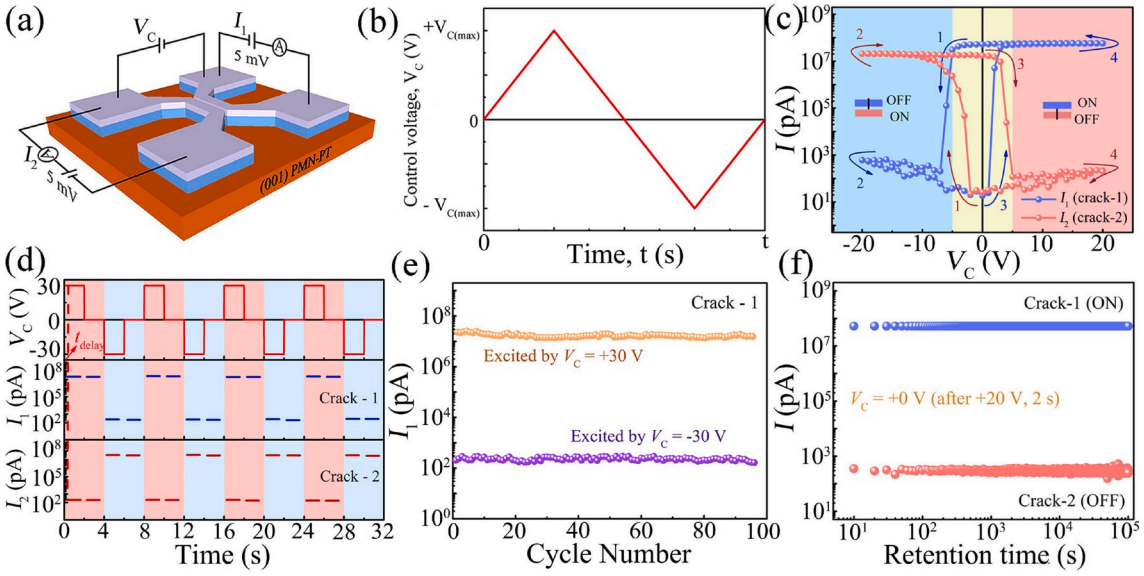

Fig. 3. Electrical performance of complementary switching. (**a**) Schematic of the device structure and the measurement setup. (**b**) The waveform of the applied V_C for generating and manipulating the cracks. (**c**) The channel current I_1 (I_2) of crack-1 (crack-2) as a function of V_C. The high and low values represent the closed and open states, respectively. The average switching voltage is about 5 V. (**d**) The repeatability test for the nonvolatile switching. The alternating voltage pulses with a magnitude of 30 V and 2 s duration were applied and the data were collected both at the voltage applied and removed. t_{delay} denotes the time delay between the voltage pulse and current switching. (**e**) The repeatability test for the crack-1. (**f**) The retention test for the states of cracks, which shows negligible change over 10^5 s.

the open to the closed. With V_C varying from – 20 V to 0 V (arrow 2 in Fig. 3c), the states of cracks remained unchanged, which agreed with the topography observation in Fig. 1. Symmetrically, under the positive V_C, the switching behavior of cracks presented an opposite variation. Note that the switching voltages have an average magnitude of 5 V. These electrical measurement results further confirm the complementary switching feature. Moreover, it can be obtained the current ON/OFF ratio is about 10^7 and the OFF-state leakage current is around 10 pA, which is close to the measurement limit of our sourcemeter. Meanwhile, we also collected the leakage current in the ferroelectric oxide between the two separated films, as shown in Fig. S4 in supporting information, whose peaks corresponded well to the switching fields in Fig. 3c. The repeatability test was also performed. The results shown in Fig. 3d were collected both when the voltage was applied and removed, demonstrating a reliable nonvolatile switching. Furthermore, no sign of fatigue was observed after applying dozens of times of alternating voltage pulses (Fig. 3e and Fig. S5) and the states of cracks could sustain more than 10^5 s without signal deterioration (Fig. 3f and Fig. S6).

2.3. Complementary inverter logic

A complementary inverter (NOT gate) is provided as an illustration, which is the basic function for constructing other complicated logic gates. Fig. 4a shows the schematic of the spatial structure of inverter. An insulating Al_2O_3 layer and conductive Pt layer are successively deposited on the MnPt layer and etched into the patterns (see experimental section 4.1). The optical image of the device and the measurement setup are shown in Fig. 4b. The voltage V_C determining the states of cracks, which is exerted on the MnPt layer, is defined as the input signal (V_{in}). As expected, the induced crack can further extend into the top Pt layer. Thereby, the output signal (V_{out}) is either pulled up to the bias electrode of V_{DD} (logic "1") or pulled down to GND (logic "0") in the top Pt layer, where the two cracks are connected in series. It should be noted that the insulating layer is used to separate V_{in} from V_{out}, which avoids the possible short circuit of V_{in} due to the temporary closing of both cracks (see discussion in supplementary note 1). Then we verified the complementary switching of cracks in the top Pt layer and the results (Fig. 4c) confirmed that the deposition of two additional layers didn't degrade the switching behavior of cracks. Fig. 4d shows the inverter voltage transfer characteristics with V_{DD} = 1.0 V. At the negative V_{in}, equivalent to logic "0", the crack-1 was open and the crack-2 was closed as previously discussed, thus the corresponding V_{out} was connected to the V_{DD} (logic "1"). On the contrary, the positive V_{in} (logic "1") resulted in V_{out} = GND (logic "0"). So the inverter logic has been implemented. In addition, the nonvolatile states of cracks after removing the applied input voltage, stored the logic computing results, which has the potential for logic-in-memory application.

2.4. Phase-field modelling

For phenomenological understanding, phase-field modelling is performed to study the domain evolution according to the time-dependent Ginzburg-Landau equation (see details in Experimental section) [17,18]. The structural analysis is also given in the supplementary note 2. A simplified two-domain configuration is considered, as shown in Fig. 5a. One polarization domain $P_4^-[\bar{1}1\bar{1}]$ can be switched to $P_1^+[111]$ by an electric field along [111], while the other one is pinned. Fig. 5b and c show the corresponding electric field and strain distributions in the domain structure, respectively. Particularly, the higher electric fields mainly distribute along the domain boundary, where the ferroelectric domain can be switched more easily. Accordingly, along the domain wall, an inhomogeneous strain is easily induced due to the domain switching and thereby the formation of crack occurs. Fig. 5e~5h show the crack evolution under the voltage pulses (Fig. 5d). Once the voltage along [111] is applied, the crack will open because the elastic energy is larger than the surface energy. However, when the voltage is along $[\bar{1}1\bar{1}]$, the crack will gradually close to reduce surface energy. Furthermore, as the voltage is applied and removed cyclically, the crack will open and close synchronously with the voltage cycles, which is consistent with the experimental results.

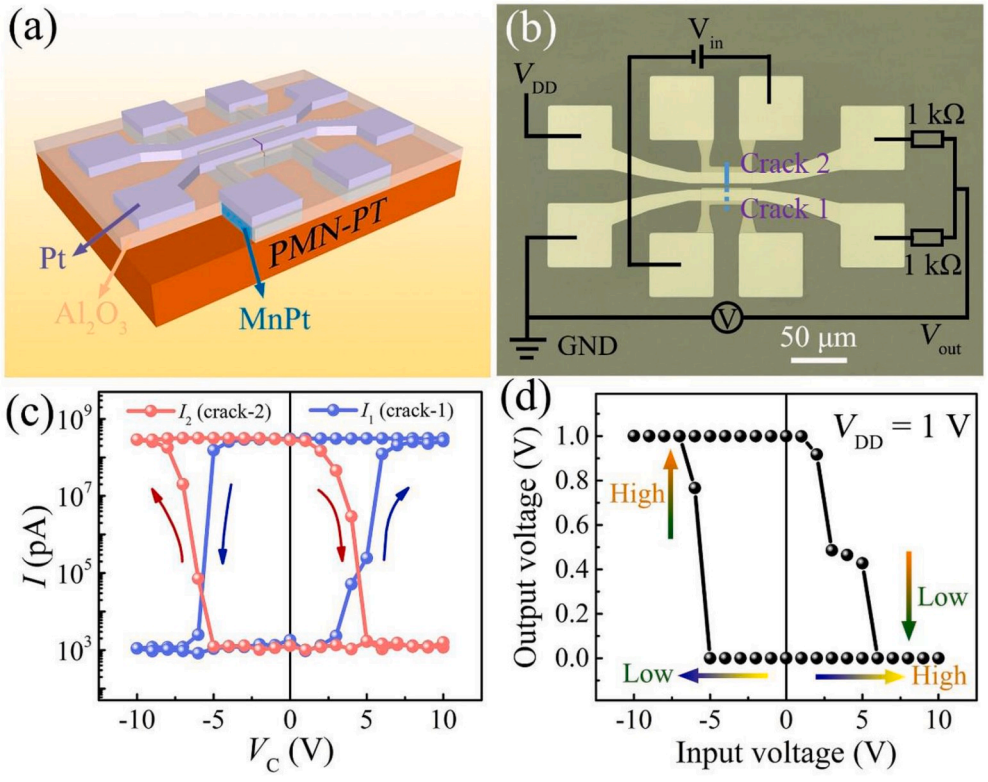

Fig. 4. Complementary ferroelectric-nanocrack inveter. (**a**) Schematic of the device structure, in which an insulating Al_2O_3 layer is incorporated between the top Pt and bottom MnPt layer. (**b**) Top-view of the fabricated device and the measurement setup. In the bottom MnPt layer, the voltage determining the states of cracks is used as V_{in}. The signal V_{DD} and GND is applied on the top Pt layer. The output node is located between V_{DD} and GND electrodes, which is connected or isolated by the cracks. The 1 kOh resistance is used for current-limiting. (**c**) The complementary switching of cracks in the top Pt layer after inserting the insulating layer. (**d**) The measured nonvolatile inverter logic function. The high (low) V_{in} results in the low (high) V_{out}.

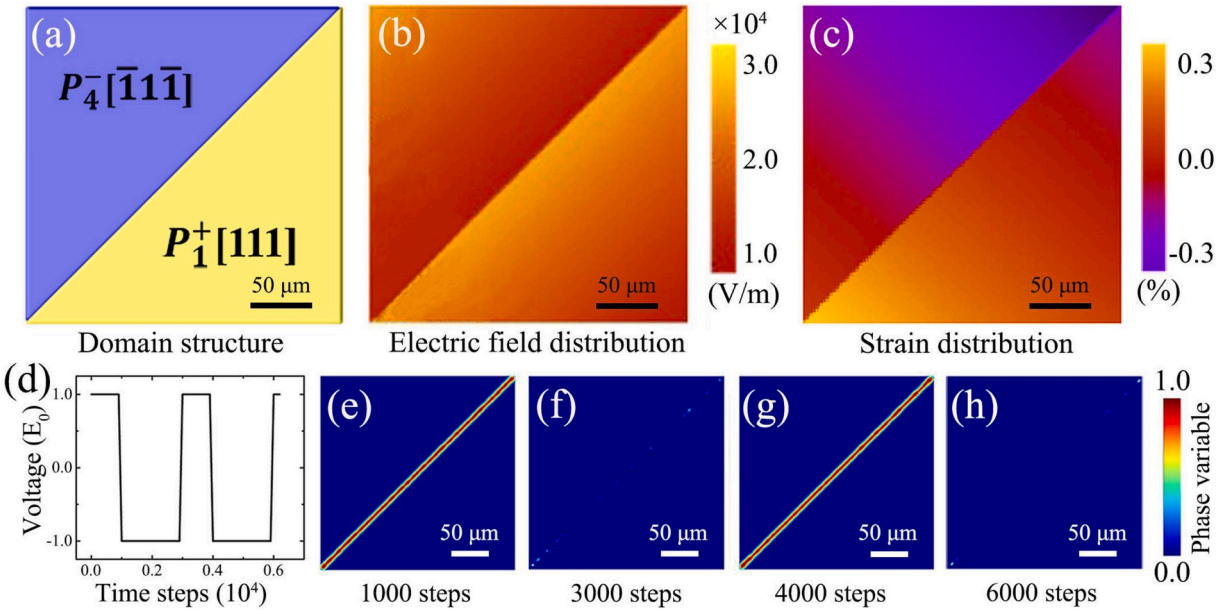

Fig. 5. Mechanism for the crack evolution from phase-field simulation. **(a)** ferroelectric domain structure, corresponding electric field **(b)** and strain distributions **(c)**, **(d)** voltage pulses inducing crack opening and closing, **(e)~(h)** the crack evolution via voltage pulses.

2.5. Reliability, power consumption and multiple logic functions

As discussed above, the crack is likely to generate along the domain wall. Therefore, the size limitation of the ferroelectric-nanocrack device is associated with the ferroelectric domain size. In our experiment, the bulk PMN-PT single crystal is used, in which the ferroelectric domains have an average 10 μm width [19]. Fortunately, as the thickness of ferroelectric oxide decreases, the domain size is also reduced [20]. As reported, the ferroelectric domain size can be as small as several nanometers, which can satisfy the sub-10 nm technology [21,22]. Moreover, the domain engineering has also been demonstrated in recent years, through which the desired domain structure can be obtained [23,24]. For example, the stripe domain structure is appropriate for forming the strictly straight crack. Such the crack has the smooth contact surface, which can avoid the destruction of the alloy thin film after massive mechanical switching and thereby improve the device endurance. On the other hand, one main reason for the failure of the mechanical switching is the surface contamination such as oxidation and hydrocarbon, which has been widely reported [25–27]. For further improving the reliability of the crack-based device, the materials both having suitable mechanical properties like MnPt and robust to the chemical reaction are required, which needs further investigation.

The changing of logic states in our device is achieved by applying a voltage to the highly insulating ferroelectric oxide, and thus the Joule heating is negligible. Specially, as the device is scaled down to the nanoscale, the operation voltage will be dramatically reduced. Considering a scaled-down device, in which each separate area has a size of 200 nm (length) × 100 nm (width) × 20 nm (height) and the gap width is 100 nm, the required switching voltage is about 5 V × (100 nm/6 μm) = 0.083 V. Such low activation voltage enables the low dynamic power consumption. The writing energy consists of two parts: one is for switching the polarization and the other for the additional surface energy. Then the calculated total writing energy per device would be 4.249 fJ (see Supplementary note 3 for the calculation process). More importantly, the leakage current across the open crack is nearly zero, thus the ultralow standby power can be obtained.

Based on the inverter logic, other logic operations such as NAND and NOR can also be implemented with the very similar manner as the CMOS technology (see Fig. S7). Furthermore, since such the logic device is actuated by the electric field and the output electrode is electrically isolated from the input one by the insulating layer, the two bias electrodes can also be used as data electrodes [28], as shown in Supplementary Fig. S8a. In terms of AND operation, one device is employed, in which IN1 is biased as - V_{DD} and IN2 is used as another input electrode, as shown in Fig. S8b. Thereby, compared with the conventional CMOS technology, the complementary ferroelectric-nanocrack logic may consume less device numbers to implement the same operation and offer the potential for the reconfigurable logic.

3. Conclusion

In summary, based on the PMN-PT/MnPt heterostructure, the complementary switching of cracks has been investigated, which is ascribed to the opposite directions of perpendicular component of electric fields in separated areas. The low ON-resistance and near-zero OFF-state leakage current, resulting in high on/off ratio, allow for the low dynamic and static power consumption. Further, we have demonstrated the ferroelectric-nanocrack-based complementary inverter logic with a non-destructive read-out process. The process-free of setting polarity of transistors allows us to fabricate the logic circuits with a simple way. We believe that this technology provides a direct pathway for constructing logic computing with low power consumption.

4. Experimental section

4.1. Thin film growth and device preparation

A 40 nm MnPt alloy thin film was deposited from a $Mn_{50}Pt_{50}$ (atomic ratio = 1:1) metallic target onto (001)-oriented $0.7PbMg_{1/3}Nb_{2/3}O_3$-$0.3PbTiO_3$ (PMN-PT) single crystal substrate (5 × 5 × 0.5 mm^3) using a radio frequency (RF) magnetron sputtering system with a base pressure better than 3.5 × 10^{-5} Pa at room temperature. The argon gas pressure was kept at 0.2 Pa. The RF source power and the sputtering time were 20 W and 12 min, respectively. After the MnPt film was deposited on the PMN-PT, it was first processed into the desired pattern as shown in Fig. 2b by photolithography and argon ion milling, with the region outside etched down to the PMN-PT substrate. For the inverter logic device, a 30 nm Al_2O_3 film was deposited successively by atomic layer deposition at 200 °C. Then the pads on the MnPt layer were etched out for applying the input signals. At last, the top Pt layer (20 nm) was

formed using the lift-off process, which was deposited by DC sputtering with a power of 20 W and argon pressure of 0.2 Pa.

4.2. Crack generation

For generating cracks, the voltage waveform as shown in Fig. 3b was applied between the two separated films. In each cycle, the voltage sequence (0→+$V_{c(max)}$→0→-$V_{c(max)}$→0) with a 5V step and 5s duration for each step was applied, where $V_{c(max)}$ denoted the maximal values of control voltage (V_c). Meanwhile, the magnitude of $V_{c(max)}$ increased with a 5V interval following the increasing cycles of voltage waveform. For our device, when $V_{c(max)}$ reached 30V, the cracks were induced.

4.3. Transport measurement

For the complementary switching of cracks measurement, as shown in Fig. 3a, Keithley 2450 (2400) sourcemeters were used to apply the constant 5 mV voltage and measured I_1 (I_2). Keithley 2410 was used to apply the control voltage V_C between the two separated areas. For the inverter logic test, as shown in Fig. 4b, Keithley 2410 was used to apply the input signal (V_{in}) and Keithley 2450 was employed to apply the V_{DD}. The nanovoltmeter (keithley 2182A) was used to measure the output signal.

4.4. Phase-field simulations

To describe the evolution of crack, a continuous phase variable η was introduced to represent the crack domain. The evolution of crack is governed by the Time-Dependent Ginzburg-Landau (TDGL) equation [17,18].

$$\frac{\partial \eta}{\partial t} = -LH(f_{elast} - f_c)\frac{\delta F_{tot}}{\delta \eta} \tag{1}$$

where L is the mobility of the crack-solid interface. $H(f_{elast}\text{-}f_c)$ is the Heaviside step function that equals 0 when $f_{elast} < f_c$, and 1 when $f_{elast} \geq f_c$. Here, f_c is a parameter for modeling the nucleation and growth of the crack. F_{tot} is the total free energy of the two-phase system that can be written as,

$$F_{tot}(\eta, \varepsilon) = \int_V \left[f_{chem} + \frac{\kappa}{2}(\nabla \eta)^2 + f_{elast}(\eta, \varepsilon)\right] dV \tag{2}$$

where κ is the gradient energy coefficient that is proportional to both the surface energy and the surface depth of the PMN-PT(001). The chemical free energy density f_{chem} is a function that has two global energy minima at $\eta = 0$, $\eta = 1$,

$$f_{chem} = w\eta^2(1-\eta)^2 \tag{3}$$

where w is the potential barrier between the two energy minima. The elastic energy density f_{elast} is calculated from the microelasticity theory [29],

$$f_{elastic}(\eta, \varepsilon) = \frac{1}{2}c_{ijkl}(r)\left(\bar{\varepsilon}_{kl} + \delta\varepsilon_{kl} - \varepsilon^0_{kl}\right)\left(\bar{\varepsilon}_{ij} + \delta\varepsilon_{ij} - \varepsilon^0_{ij}\right) \tag{4}$$

where $c_{ijkl}(r)$ is the spatially variant elastic stiffness tensor, which can be described as,

$$c_{ijkl}(r) = c^{PMN-PT}_{ijkl}(1 - h(\eta)) + c^{crack}_{ijkl}h(\eta) \tag{5}$$

where h(η) = η^3(6η^2-15η+10) is the interpolating function that makes the elastic constant inhomogeneous in the system. $\bar{\varepsilon}_{ij}$, δ_{ij} andε^0_{ij} represent the homogeneous strain, heterogeneous strain, and the stress-free transformation strain, respectively. The homogeneous strain describes the average deformation of the system and have the relation,

$$\int_V \bar{\varepsilon}_{ij} dV = 0 \tag{6}$$

The heterogeneous strain can be expressed as,

$$\delta\varepsilon_{ij}(r) = \frac{1}{2}\left[\frac{\partial u_k(r)}{\partial r_l} + \frac{\partial u_l(r)}{\partial r_k}\right] \tag{7}$$

where u_i(r) denote the ith component of displacement.

The stress-free transformation strain describes the influence of the local polarization on the local strain in a ferroelectric material and is given by,

$$\varepsilon^0_{ij} = Q_{ijkl}P_kP_l \tag{8}$$

where Q_{ijkl} is the electrostrictive stiffness tensor; P_k, P_l represent local polarization vectors. In the two-domain configuration, we have ε^0_{12} = 0.2% in theP_1^+ domain, which will make a crack to form in the domain. To get the strain distribution, the mechanical equilibrium equation is solved at each step,

$$\frac{\partial \sigma_{ij}}{\partial x_j} = 0 \tag{9}$$

where σ_{ij} represents the local elastic stress. Due to the inhomogeneous elastic stiff tensor, the mechanical equilibrium equation can be solved using a Fourier-spectral iterative perturbation method [30]. In our simulation, the system is two-dimensional and the grid is 256$\triangle x$ × 256$\triangle y$, with $\triangle x = \triangle y = 1$ μm. The elastic stiff tensor is taken from Ref. [31]. As an approximation, the surface energy of (001) $BaTiO_3$ is used here to represent the PMN-PT (001) [32]. The critical elastic energy is chosen as 10 MJ/m^3 [13].

Author contributions

L.Y. and Z.G. conceived and designed this project. Z.G. and Q.L. performed the sample growth, device fabrication and electrical measurements with the assistance from S.Z. and Q.Z. Q.L. performed the SEM measurements. Z.G. contributed to the COMSOL simulations. F.S. performed the PFM measurement. H.H., X.S., Y.J. and L.Q.C. contributed to the phase-field simulations. Z.G., Q.L., M.S. and L.Y. wrote the manuscript with the help from all other authors. All authors discussed the results and commented on the manuscript.

Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

CRediT authorship contribution statement

Zhe Guo: Conceptualization, Methodology, Validation, Investigation, Writing - original draft, Funding acquisition. **Qiang Luo:** Validation, Investigation, Data curation. **Houbing Huang:** Methodology, Software, Writing - review & editing. **Shuai Zhang:** Software. **Xiaoming Shi:** Methodology, Software. **Fei Sun:** Investigation. **Yanzhou Ji:** Methodology, Software. **Qiming Zou:** Investigation. **Min Song:** Writing - review & editing, Funding acquisition. **Xiaofei Yang:** Resources. **Deyang Chen:** Validation, Resources, Writing - review & editing, Funding acquisition. **Jeongmin Hong:** Writing - review & editing. **Long-Qing Chen:** Methodology, Software. **Long You:** Conceptualization, Resources, Writing - review & editing, Supervision, Project administration, Funding acquisition.

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Appendix A. Supplementary data

Supplementary data to this article can be found online at https://doi.org/10.1016/j.nanoen.2020.104871.

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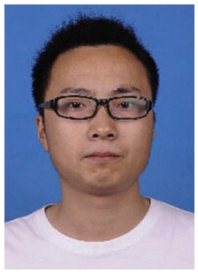

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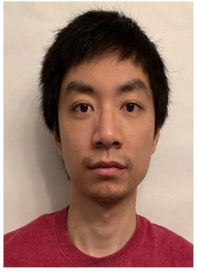

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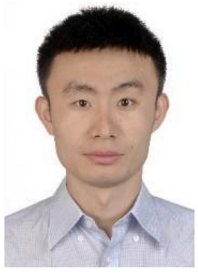

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