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Ferroelectric-Nanocrack Switches for Memory and Complementary Logic with Zero Off-current and Low Operating Voltage

*Zhe Guo, Yaodong Guan, Qiang Luo, Jeongmin Hong, and Long You**

Ferroelectric devices have attracted intensive research in memory and logic applications due to their non-volatility, scalability, and energy efficiency. As an emerging technology, the ferroelectric nanocrack device offers a simple and efficient way to manipulate the device resistance states with a high on/off ratio. Meanwhile, its complementary switching enables the construction of logic gates with a similar way as the complementary metal oxide semiconductor (CMOS) technology. Here, it is demonstrated that the memory and logic functions can be realized by the same device structure with superior electrical performance, such as reliable metallic on-state contacts, zero off-state leakage current, and wide working temperature range (–110 to 150 °C). Moreover, the scaling performance has been investigated and the operating voltage can be reduced to average 2.5 V with device scaling down to sub-micrometers. Following the scaling rule, the operating voltage can shrink largely to sub-1 V at 100 nm nodes. In addition, the logic gates including NOT, 2:1 MUX, AND, and OR functions have been experimentally demonstrated. It is believed that this work can expand the scope of ferroelectronics and be applicable to logic-in-memory computing in the future.

1. Introduction

Ferroelectric oxides utilize polarization switching to construct functional devices by voltage-control, offering great advantages in non-volatility, scalability, and energy-efficiency.[1,2] To date, diverse ferroelectric devices have been developed and extensively investigated including ferroelectric capacitor memory,[3] ferroelectric tunnel junction,[4,5] ferroelectric field effect transistor (FET),[6–8] negative capacitance FET[9,10] and domain wall devices.[11,12] The non-destructive readout of polarization states, which however is an obstacle in the initial ferroelectric capacitor technology, has become readily accessed in other ferroelectric technologies and thereby leads to higher reliability. In addition, the discovery of ferroelectric materials that are compatible with complementary metal oxide semiconductor (CMOS) manufacturing processes, such as hafnium oxide, has largely promoted the development of ferroelectric devices.[13,14] The ferroelectronics shows promise as a universal alternative for memory and logic computing in modern electronics. In particular, condensing the memory and logic functions into one device is highly desired for logic-in-memory computing. As a representation, ferroelectric FET, which contains a ferroelectric layer in the dielectric stack of metal-oxide-semiconductor FET (MOSFET), can act as either the memory or logic devices.[1]

Recently, the discovery of ferroelectric nanocrack device gives rise to a new way to exploit the polarization switching,[15–17] offering another non-destructive readout approach. Remarkably, such device exhibits superior performance in both on and off states compared to other ferroelectric devices, with metallic contacts at its on state and zero off-state leakage current. Moreover, a complementary switching in this ferroelectric nanocrack device, with a similar operation manner as the CMOS technology, has also been revealed to enable the functionality for digital computing.[16] As data-intensive applications such as Artificial Intelligence and the Internet of Things become more and more popular and important, the energy-efficient hardware and architecture are required.[18,19] The same basic device structure for both logic computing and data storage can largely save the energy and time consumption of data movement between the separate processing and storage units in von Neumann architecture. Thus, it is viable and urgent to merge the logic and memory functionalities of ferroelectric-nanocrack at the single-device level. On the other hand, the study on the ferroelectric nanocrack-based devices is still at the infant stage and the route to real application is challenging. For instance, the investigations of performance at scaled dimensions are still lacking. Moreover, the high operating voltage (>5 V) has posed a major obstacle for the reduction of dynamic power consumption, which are crucial for applications.

In this work, using the same basic device structure, the memory and logic functions have been demonstrated. The performance of one-crack based memory device was firstly explored, with reliable metallic contacts at on state, low leakage current about 10 fA μm^{-1} and wide working temperature range. Specially, we experimentally investigated the scaling of

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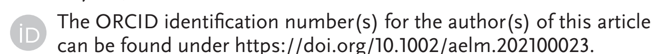
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operating voltage with a featured gap length (L_g) varying from micrometers to sub-micrometers. An average 2.5 V operating voltage was acquired with L_g = 300 nm and sub-1 V could also be obtained obeying the scaling rule through simulation. The zero off-state leakage current and low operating voltage enables the construction of energy-efficient devices. Then, the double-cracks based logic devices were researched and the logic gates including NOT, 2:1 MUX, AND, and OR functions were experimentally demonstrated. We believe that our work can advance the development of ferroelectric nanocrack devices and expand the scope of ferroelectronics.

2. Results and Discussion

The appearances of cracks in electronic devices are always destructive due to its irreversibility. Here, the nanocrack induced in ferroelectric oxides that we employed for functional devices can be electrically switchable.[20] In previous works,[16,20] it has been theoretically and experimentally verified the nanocrack behaviors are strictly correlated with surrounding ferroelectric domain switching. Along the domain boundary, a crack may form to release the elastic energy produced from the domain switching. The tensile and compressive strain accompanied by the domain switching causes opening and closing of nanocracks. **Figure 1**a shows the schematic of one-crack based memory device and its working principle. The device is comprised of ferroelectric oxide and metallic thin film, where the film is etched into parallel strips with a gap length L_g. The voltage V_G applied across the parallel strips, which drives the domain switching underneath the thin film, is responsible for inducing the crack (see details in methods) and manipulating the crack switching. The crack can extend into the metallic thin film and also reversibly switch in the film. V_{DS} serves as the reading voltage to detect the device resistances decided by the states of crack. When the crack is open (bottom left panel of Figure 1a), a nanoscale air gap is formed and concomitantly the current path is cut off, leading to the high resistance state (HRS). The opposite V_G enables the closing of crack (bottom right panel of Figure 1a) and the current path recovers, causing the low resistance state (LRS).

Figure 1b illustrates the crack morphology (top view) of a real device captured through scanning electron microscope (SEM). This device consists of (001)-$Pb(Mg_{1/3}Nb_{2/3})_{0.7}Ti_{0.3}O_3$ (PMN-PT) substrate/MnPt (40 nm)/Pt (5 nm) with L_g = 6 µm (see fabrication details in Experimental Section). The PMN-PT used in our work, which is in the region of morphotropic phase boundary (MPB), has complicated ferroelectric domains[21] and the MnPt film has moderate mechanical properties.[20] The top right panel of Figure 1b shows the SEM image of open-state of crack,

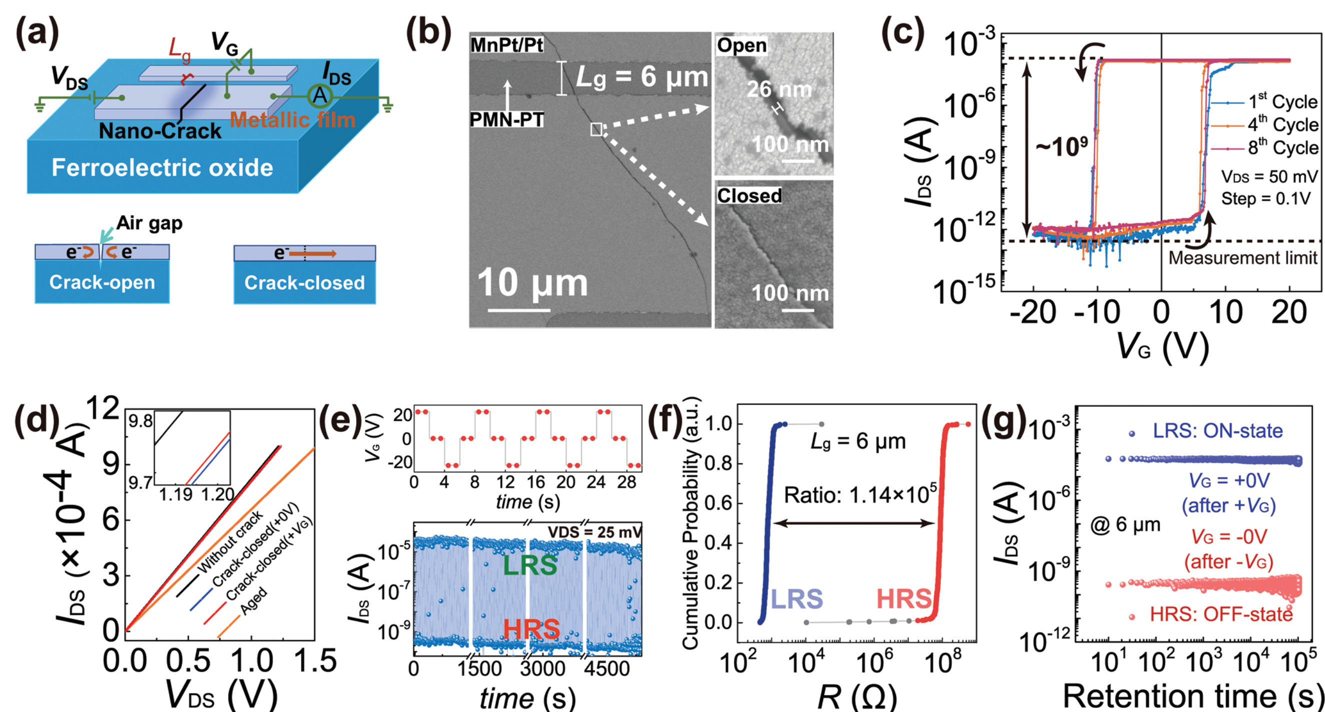

Figure 1. a) Schematic of single-crack based memory device and its working principle for manipulating the device at HRS (bottom left) or LRS (bottom right) states. b) The left panel shows the SEM image of full view of crack morphology (open state) in the device with L_g = 6 µm. The right panel illustrate the SEM images of enlarged view of local crack (corresponding to the solid line rectangular area in the left panel) when it is open (top right) or closed (bottom right). The width of the metal film strip is 30 µm here. c) The measured I_{DS}-V_G loops for the switching of crack with a 0.1 V step and V_{DS} = 50 mV. V_G sweeps from +20 to −20 V and then back to +20 V. d) I_{DS}-V_{DS} loops before (black line) and after the crack (blue line for V_G = 0 V and red line for V_G = 20 V) is induced. The orange line represents the aged crack. The inset shows the enlarged view where V_{DS} ranges from 1.185 to 1.2025 V. e) The repeatability test under voltage pulses (±20 V) with a 2 s duration as shown in the top panel. The data were collected with a 1 s interval (indicated by the red dots in the top panel) and V_{DS} = 25 mV. f) The distributions of HRS and LRS extracted from the repeatability tests. g) The retention test in LRS state and HRS state, respectively.

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which has a width of 26 nm on the film surface. The bottom right panel presents the image when the crack is closed. Then we measured channel current I_{DS} as a function of V_G through sweeping V_G with a constant V_{DS}. As shown in Figure 1c, a hysteresis loop is observed, which should be due to the non-volatile 109° switching of ferroelectric domain.[22] Abrupt switching occurs once V_G reaches the critical switching fields, which are average 10 V here for such device. At a small V_{DS} (50 mV), a high on/off current ratio (≈10^9) has been achieved with ultralow off-state current (about 10 fA μm^{-1}, the width of the strip is 30 μm) that is close to our equipment measurement limit. After several cyclic measurements, the switching characteristics maintain stable, as revealed by the results in Figure 1c. The switching loops with different scanning steps have also been performed, as shown in Figure S1 (Supporting Information), which has negligible effect on the switching performance. In order to confirm the metallic contacts during the crack was closed, we compared the on currents before and after the crack was induced. As shown in Figure 1d, the linear relationships between I_{DS} and V_{DS} demonstrate an ohmic contact. The on currents without crack are very slightly higher than the ones with crack (inset of Figure 1d), indicating the excellent metallic contacts even after the crack is induced. Moreover, the reliable non-volatile control is also confirmed by the same on currents with V_G = 0 V (blue line) and V_G = 20 V (fully-on state, red line). The orange line shows the performance of on currents after two months, which decrease largely compared to pristine one. We attribute this to the oxidation and contamination of contact surfaces during a long time. Furthermore, the repeatability test was performed (Figure 1e) and our device still presented good performance even after more than 10^3 times measurements under voltage pulses. The distributions of HRS and LRS extracted from the repeatability tests are shown in Figure 1f, presenting relative stable states and wide resistance window. The gray dots in Figure 1f correspond to those values between HRS and LRS in Figure 1e, which appears randomly and needs further device optimization. Figure 1g illustrates the retention test results and the states of our device after removing V_G maintained stable during the measurement time.

Figure 2 shows the I_{DS}-V_G loops collected under different temperatures. At low temperature range (160–280 K), the switching voltage presents a tendency to slightly decrease with increasing temperature. This may be related to the fact that the switching of the ferroelectric domain is affected by temperature.[23] At high temperature range (300–440 K), I_{OFF} slightly increases compared to the ones at low temperatures, which could be related to the increase in thermal noise. However, when the temperature is higher than 420 K, the switching behavior of crack gradually disappears with the increase of temperature that may exceed the Curie temperature of PMN-PT.[24] Therefore, our device exhibits a wide working temperature range from –110 to 150 °C.

Next, we investigate the characteristics of device at scaled dimensions. We have fabricated two scaled devices with different L_g (300 and 500 nm). **Figure 3**a and Figure S2 (Supporting Information) show the SEM images of devices with L_g = 300 and 500 nm, respectively, which are fabricated through electron beam lithography and lift-off process. The corresponding I_{DS}-V_G loops are shown in Figure 3b. As expected,

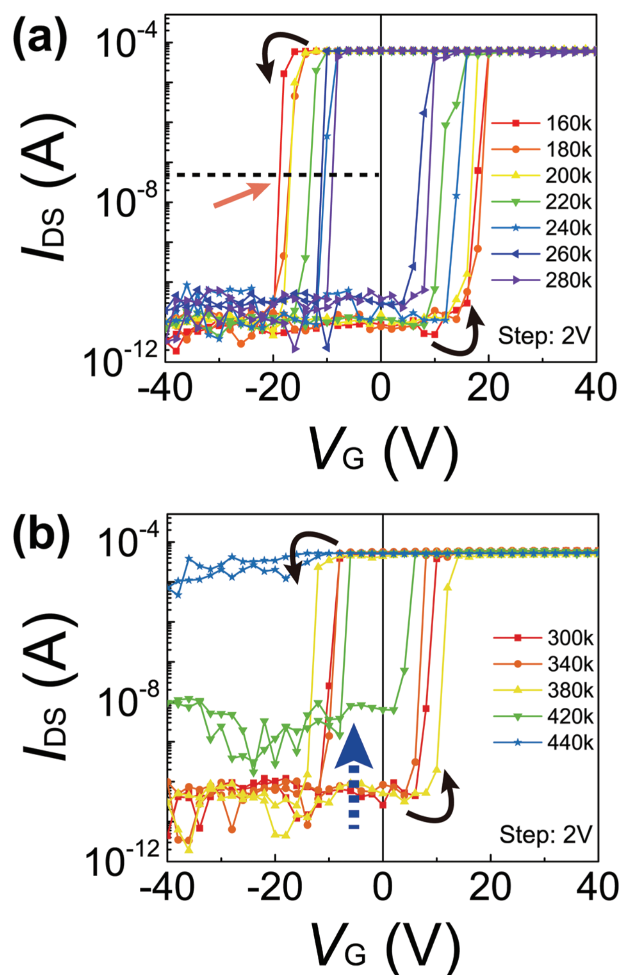

Figure 2. The switching of crack under a) low a) and b) high temperatures. The sweep of V_G has a 2 V step.

the switching voltages have been largely reduced to average 3.5 V (for L_g = 500 nm) and 2.5 V (for L_g = 300 nm). Figure 3c and Figure S3 (Supporting Information) show the repeatability test results for the devices with L_g = 500 and 300 nm, respectively, indicating that the device still has good repeatability even at scaled dimensions. The distributions of HRS and LRS (Figure 3d and Figure S4, Supporting Information) demonstrate wide resistance window for the nanoscale devices. In addition, the nanoscale device also presents similar switching performance under different temperatures as the one with L_g = 6 μm, as shown in Figure S5 (Supporting Information). Moreover, Figures S6 and S7 (Supporting Information) show the retention test results for the nanoscale devices with L_g = 500 and 300 nm, respectively.

In order to confirm the stability of operating voltages for devices with different L_g, we have carried out cyclic tests of switching loops for each device and conducted the statistic analysis (**Figure 4**a–c). Specifically, the forward switching voltages (from I_{ON} to I_{OFF}) and backward switching voltages (from I_{OFF} to I_{ON}) are extracted from the loops and we record the counts of different voltages. Then the Gauss fitting is used to estimate the stability. As a result, the distribution of the forward

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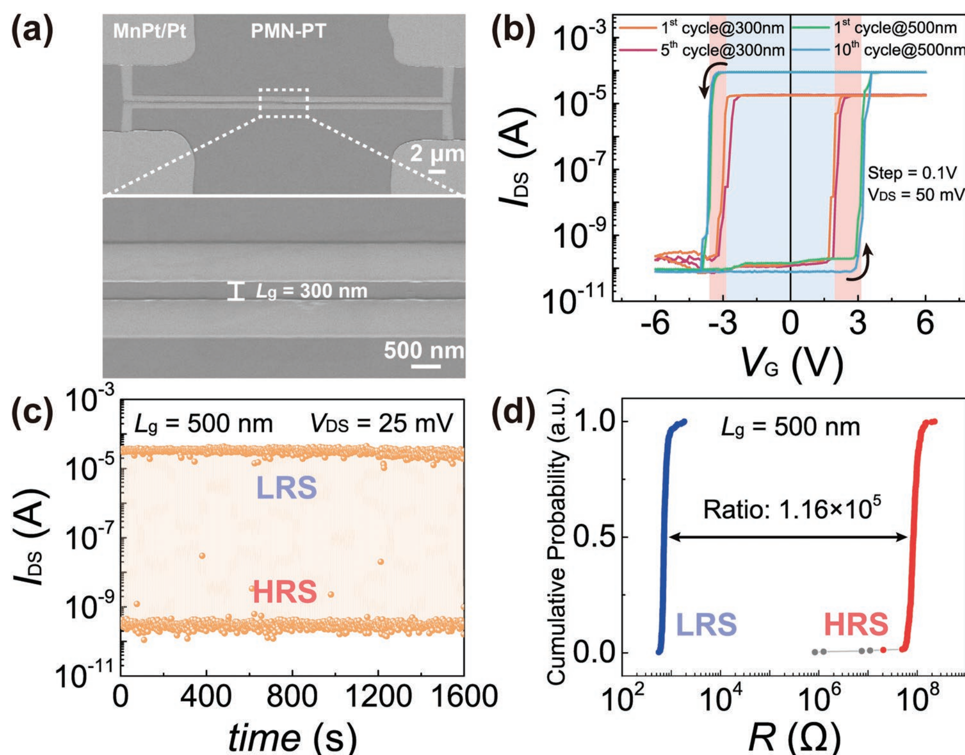

Figure 3. a) The SEM images of full-view (top) and enlarged view (bottom) of device with $L_g = 300$ nm. b) The measured I_{DS}-V_G loops corresponding to the device with $L_g = 300$ and 500 nm. c) The repeatability test results for the device with $L_g = 500$ nm, $V_{DS} = 25$ mV. d) The distributions of HRS and LRS for device with $L_g = 500$ nm.

switching voltages follows a Gaussian distribution that is centered at 10.50447 V with a standard deviation of 0.08647 V for L_g = 6 µm, as shown in Figure 4d, which has a small deviation and thus indicates the stability of our device. Figure 4e,f show the distributions of L_g = 500 and 300 nm, respectively, which also present small deviations. In addition, the backward switching voltages are also stable under cyclic tests (see Figure S8, Supporting Information).

This scaling rule is simply due to the fact that the ferroelectric domain switching is determined by the applied electric field that is dominated by not only the magnitude of voltage but also the distance (L_g). The COMSOL software is used to study the further scaling performance, as shown in Figure 4g. From the simulation results of L_g = 6 µm and 300 nm, one can see that the operating voltages obtained from experimental results V_G = 10.5 V (for L_g = 6 µm) and 2.5 V (for L_g = 300 nm) cause the similar z-component of electric field (E_Z)magnitudes in the devices. Therefore, relying on the electric field distribution, it is roughly estimated that just a very small operating voltage (V_G = 0.75 V) is needed for L_g = 100 nm. The extracted operating voltages for different L_g (ranging from 100 nm to 6 µm) are summarized in Figure 4h. As L_g is scaled down, the operating voltage rapidly decreases. Then we quantitatively estimate the writing power consumption for a scaled device with L_g = 100 nm. Given that the device has a 200 nm(length) × 100 nm(width) × 40 nm(thickness) electrode where the crack is induced, the writing energy per bit is calculated to be 10.25 fJ, which consists of polarization switching energy and surface energy (see details in Supporting Information).

Figure 4i illustrates our proposed single device and devices array design for further scaling. The minimum single device structure is potentially scalable down to dimensions with only two domains (indicated by the orange arrow in Figure 4i) since the crack is mostly possible induced along the domain boundary as discussed in previous works.[16,20] Note that the bulk PMN-PT substrate used in our experiments has an average 10 µm domain sizes,[25] which limits the reduction of device longitudinal dimensions shown in Figure 3a. However, the domain sizes can be largely reduced even to sub-10 nm, with the decrease of ferroelectric oxide thickness, offering great potentials for scaling down.[26,27] On the other hand, in order to improve the reliability at scaled dimensions, the regular strip domains are highly preferred to form the nano-crack with smooth surfaces,[28] which can effectively avoid the destruction of films from mechanical contacts.

Then, we demonstrate the logic gates based on the complementary switching of double-cracks. As schematically shown in **Figure 5**a, the basic structure is the same as the previous one for memory, but here we focus on the correlation of two cracks induced in the separated thin film zones, where each zone has one crack. Under the application of V_G with different polarities, one can always find that one crack is open and the other one maintains closed, presenting a complementary characteristic. As the SEM image shown in Figure 5b, the two cracks clearly illustrate the opposite states. Such phenomenon comes from the complementary distributions of E_Z within the device, which can be easily understood through splitting the electric fields as shown in Figure S9 (Supporting Information). The simulations

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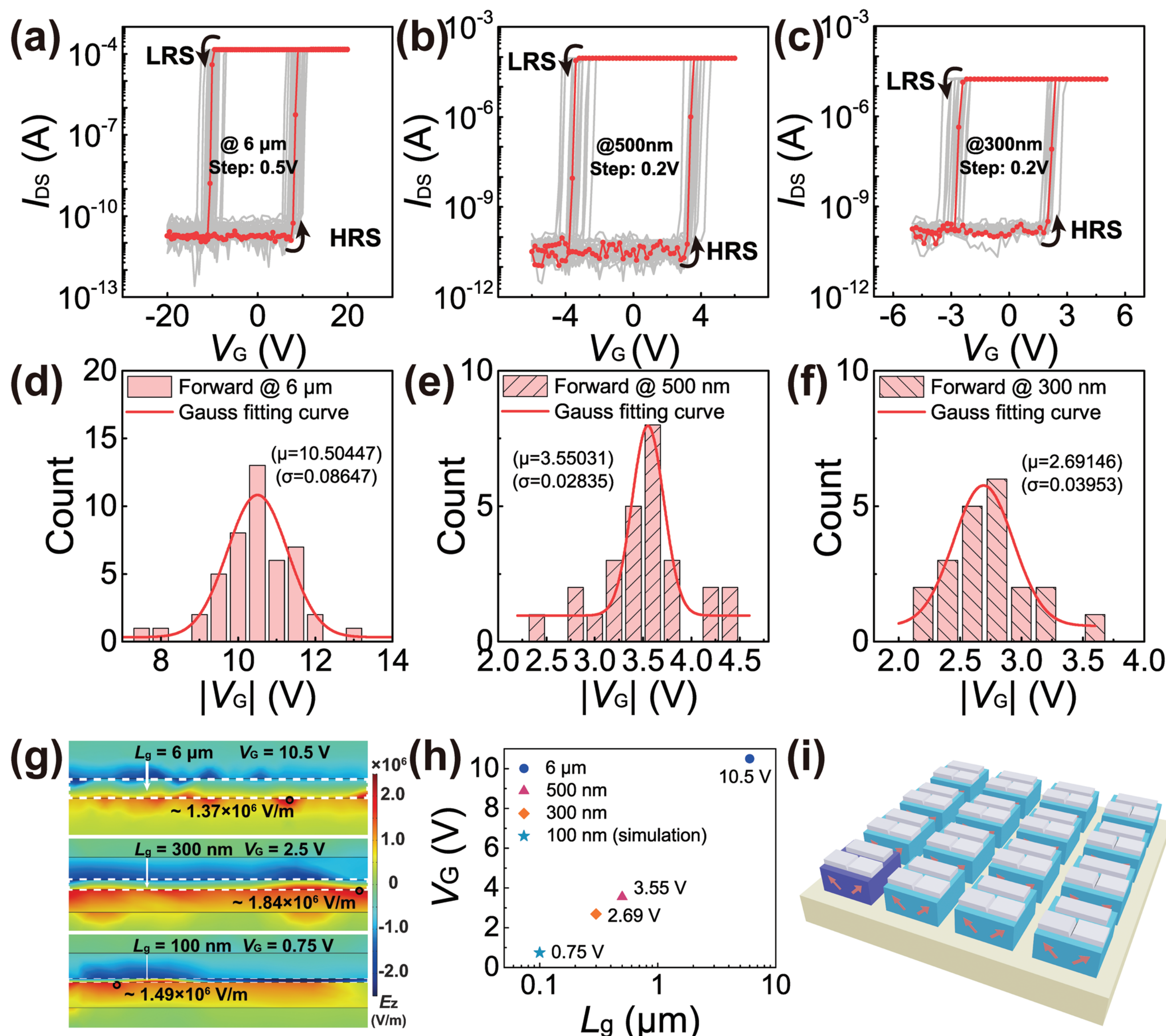

Figure 4. a–c) Multiple switching loops for the device with $L_g = 6$ μm, 500 nm, and 300 nm, respectively. d–f) The distribution of the forward switching voltages for the device with $L_g = 6$ μm, 500 nm, and 300 nm, respectively. g) The E_Z distributions under operating voltages for devices with different L_g using COMSOL software. The labeled electric fields represent the values of black circle location. h) The extracted operating voltages for different L_g (ranging from 100 nm to 6 μm). i) Design of single device and devices array for further scaling. The arrows depict the polarization directions of ferroelectric domains.

in Figure 4g also confirm the complementary distributions, where the red and blue colors represent the positive and negative electric fields, respectively. The complementary switching behavior here resembles the operating process of CMOS technology comprising PMOS and NMOS. The formation of PMOS and NMOS needs a complicated ion implantation process, whereas it is not required in our device since the complementary characteristics appear once the cracks are generated.

Figure 5c shows the I_{DS}-V_G loops of double cracks collected simultaneously. The electrical performance solidly confirms the complementary switching. The positive V_G leads to HRS of crack-1 and LRS of crack-2, while the negative V_G reverses their states. We repeatedly measured the complementary switching using the voltage pulses that are shown in Figure 1e, which also exhibits good reliability after hundreds of times (Figure 5d). From the enlarged view (top of Figure 5d), one can distinctly see the complementary property and nonvolatile control. The slight difference in LRS of two cracks may originate from the geometry variations of electrodes from fabrication process and the different contact resistances of wire bonding for tests.

Finally, we used the complementary switching to construct logic gates. An insulating (Al_2O_3) and a top metal (Pt) layer are deposited successively on top of MnPt layer, as schematically shown in Figure 5e. The added insulating layer is mainly used to isolate the output signal from the input one such that the logic device has a high input resistance. Thus, the output signal can

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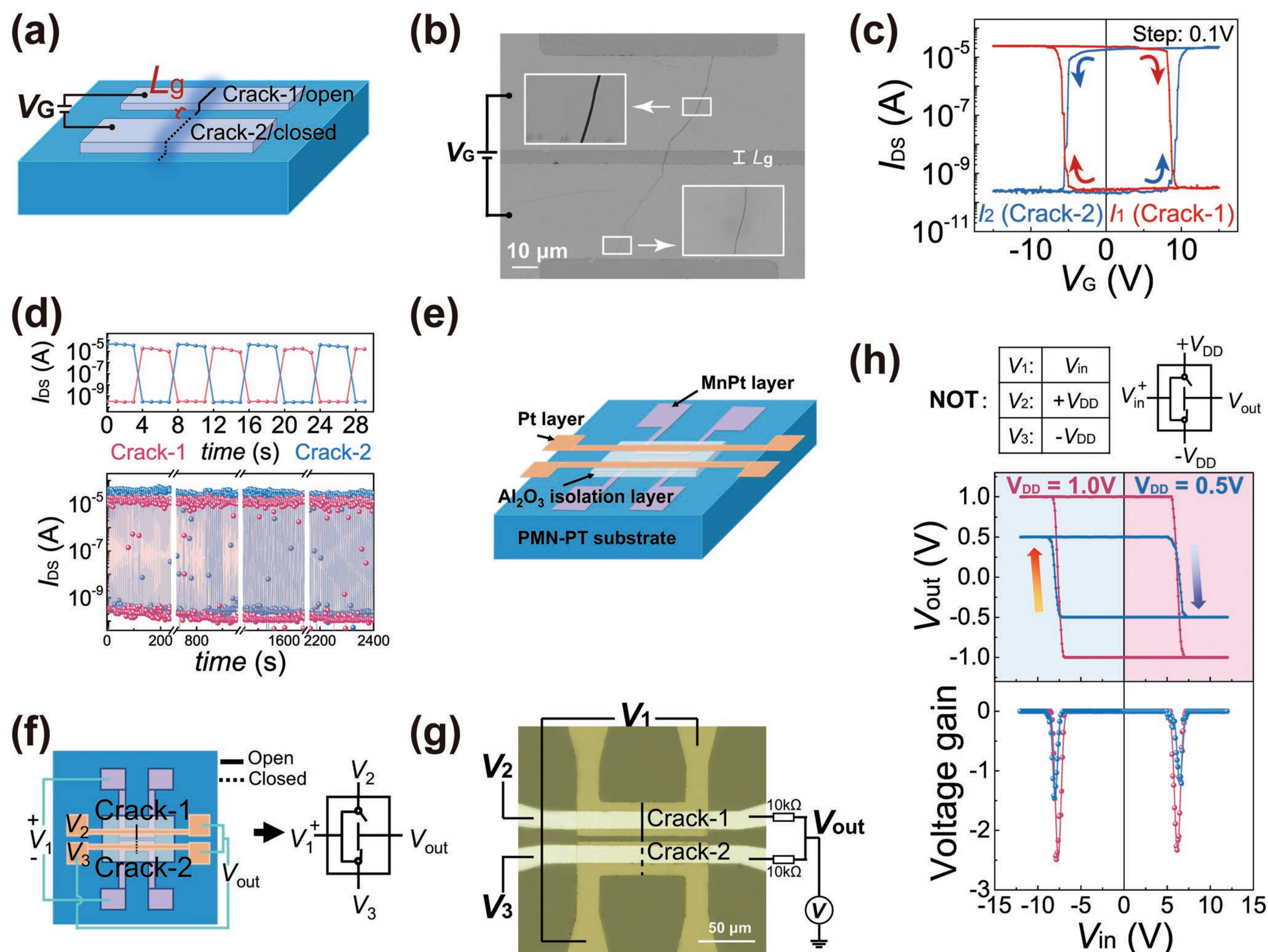

Figure 5. a) Schematic of complementary switching of double-cracks. b) The SEM images of crack morphology for the crack-based logic devices with $L_g = 6$ μm, showing opposite states of cracks. The white rectangular areas illustrate the enlarged view. c) The electrical performance for the complementary switching of cracks with a 0.1 V step. The red and blue loops represent for crack-1 and crack-2 shown in Figure 3a, respectively. d) The repeatability test for the complementary switching of cracks under voltage pulses that are the same as the ones shown in Figure 1e. The top panel presents the enlarged view from 0 to 30 s. e) The 3D structure schematic of device for constructing logic gates, where the Al_2O_3 and Pt layers are added successively. f)The schematic of circuit diagram and corresponding circuit symbol. g) The measurement setup and optical image of a fabricated logic device. h) The circuit setup and transfer characteristics of inverter logic with different V_{DD}.

serve as the input of other devices, enabling to construct cascadable logic gates. Figure 5f shows the top view schematic and corresponding circuit diagram. The voltage V_1 applied on the MnPt layer is responsible for the actuation of cracks switching, which can extend through the Al_2O_3 and Pt layers. The top metal layer serves as the signal path, whose connection and disconnection are determined by the crack states. These two paths are linked in series and thereby the output connects to either one. It can be found the signals applied on the top layer are independent from the one on the bottom layer, offering more flexibility for the circuit design compared with CMOS technology. The optical image of one fabricated device is shown in Figure 5g.

As the building block of digital logic computing, the complementary inverter was demonstrated. Top panel of Figure 5h shows circuit diagram for NOT/inverter gate. The two ends of signal paths on the top layer are connected to $+V_{DD}$ and $-V_{DD}$, respectively. Under the actuation of V_{in}, the V_{out} connects to either $+V_{DD}$ or $-V_{DD}$. The positive V_{in} results in the open of crack-1 and closing of crack-2, leading to $V_{out} = -V_{DD}$. The negative V_{in} causes $V_{out} = +V_{DD}$. The transfer characteristics of the inverter and corresponding gain values are shown in bottom panel of Figure 5h. The low-level voltage can ideally reach $-V_{DD}$, indicating the good cut-off characteristic of crack. Moreover, we perform different V_{DD} and find that the switching voltage (define when $V_{out} = 0$ V) here is independent of applied V_{DD}, which differs from the CMOS inverter. It should be noted that the input-output characteristic we demonstrate here is not a rail-to-rail operation, where the input voltage to drive the switching of crack is relatively high. In our experiments, it is observed that with the increase of V_{DD}, the film will be broken. We attribute this to the breakdown of the deposited insulating layer or the air gap of crack by the high voltage. As discussed above, this issue can be further optimized through reducing the device dimensions. The

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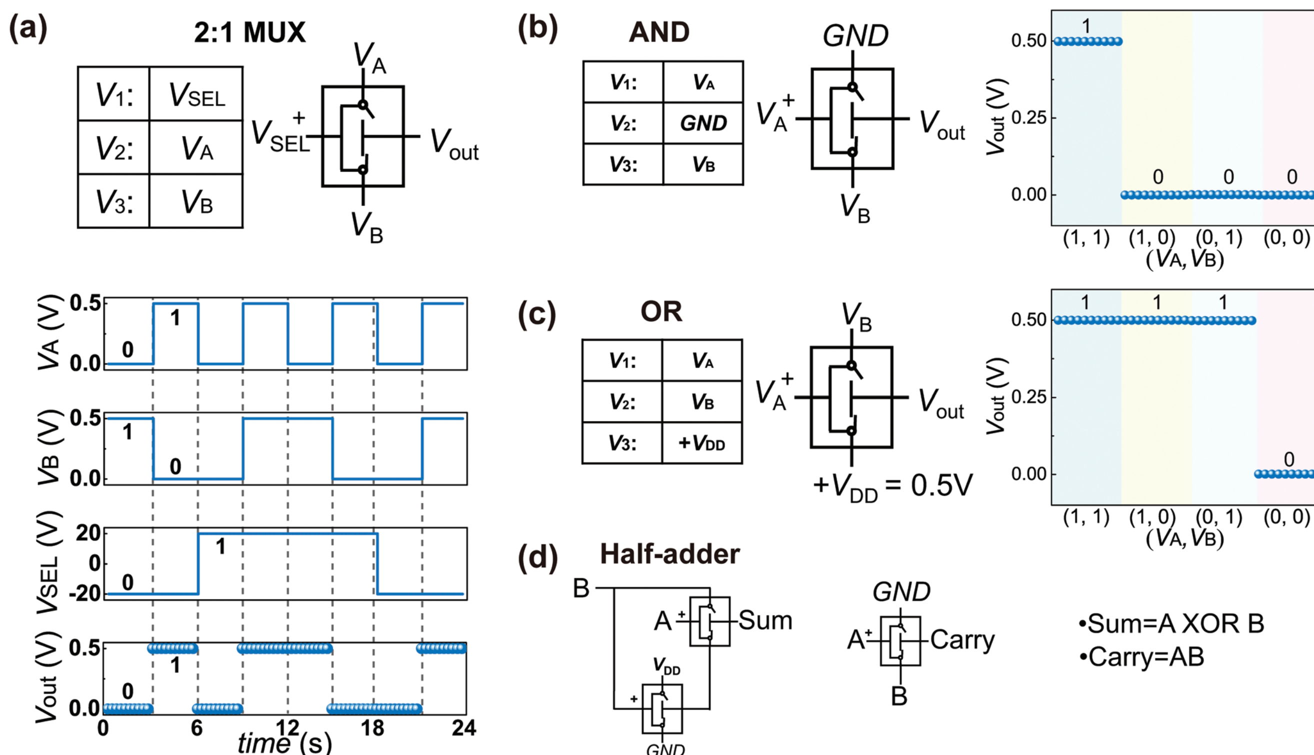

Figure 6. a) The circuit diagram and output characteristics for 2:1 MUX. b) The circuit diagram and output characteristics for AND gate. c) The circuit diagram and output characteristics for OR gate. d) The circuit diagram for half-adder logic.

ferroelectric material with a lower switching field can also be employed to address this issue. Then, the gain values will also be vastly improved.

Our nanocrack-based devices behave like the nanoelectromechanical (NEM) switches as discussed in our previous work,[15] and thereby can be adopted to construct complex logic gates with the similar manner as NEM switches, which consume less device counts compared with conventional CMOS technology.[29,30] From above discussions about complementary switching process, it is clear our device is readily applicable for signal path selection. **Figure 6**a shows the circuit diagram and output characteristics of 2:1 MUX, where V_{SEL} is used to decide which path is selected. When V_{SEL} is set as negative voltage (logic 0), the output connects to V_A, and thus it can be seen the output waveform is consistent with the one of V_A (Figure 6a). Upon V_{SEL} switches to positive voltage (logic 1), the variations of V_{out} coincides with V_B at once. In order to implement 4:1 MUX, as shown in Figure S10 (Supporting Information), three basic elements (one element contains two nanocracks) are sufficient while 26 MOSFETs are required using CMOS technology.[29] Further, as illustrated in Figure S11 (Supporting Information), a 2N:1 MUX can be easily implemented by $N(N + 1)/2$ elements, in which the outputs of previous stage are connected to the inputs of next stage. The circuit diagrams of AND and OR logic gates and corresponding output characteristics are shown in Figure 6b,c, respectively. For AND logic, the logic 1 (higher than 0 V here) output only appears when both inputs (V_A and V_B) are at high voltage levels (Figure 6b) and at this point the output connects to V_B. As for OR logic, the output maintains logic 1 if either of inputs is at high voltage level (Figure 6c). Moreover, multiple-inputs AND or OR logic can also be readily constructed through feeding the output of one element to the input of other one, as shown in Figure S12 (Supporting Information). N-inputs AND or OR logic only need N-1 basic elements. Furthermore, the half-adder, as the basic building block of modern processors, can be implemented by only three elements in total (Figure 6d), offering less device counts compared with CMOS technology (Figure S13, Supporting Information). The full basic logic functions by the nanocrack devices have been summarized in Figure S14 (Supporting Information).

3. Conclusion

In this work, we have demonstrated the memory and logic functions in a single ferroelectric-nanocrack device. The reliable metallic contacts at on state have been confirmed through comparing the conductance before and after the nanocrack is induced. The zero off-state leakage current was realized due to the ideal cut-off characteristic of nanocrack. Therefore, at a small $V_{DS} = 50$ mV, a high on/off ratio ($\approx 10^9$) has been achieved. In addition, at sub-micrometer scaled dimensions, the low operating voltages have been observed. The zero off-state leakage current and low operating voltage are responsible for the low static and dynamic power consumption, respectively, enabling the construction of energy-efficient devices. On the other hand, the spontaneous complementary switching offers a simple way to construct logic gates. Logic gates of NOT, 2:1 MUX, AND and OR based on crack switches have obtained good output characteristics. We believe that the nanocrack based devices offer

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a new energy-efficient hardware platform for logic-in-memory applications.

4. Experimental Section

Thin Film Deposition and Device Fabrication: 40 nm $Mn_{50}Pt_{50}$ thin films were deposited on the PMN-PT substrate by radio frequency (RF) sputtering at room temperature. The RF power was 20 W, argon gas pressure was 0.2 Pa and the sputtering time is 12 min. Then 5 nm Pt layer was deposited on top of MnPt using direct current sputtering. The device patterns with L_g = 6 μm were fabricated through photography and argon ion milling while the devices with L_g = 300 and 500 nm were patterned through electron beam lithography and lift-off process. For the logic device, the insulating layer Al_2O_3 (30 nm) were grown by atomic layer deposition at 200 °C. Then the Al_2O_3 film on the electrode areas of MnPt/Pt was etched out for electrical measurement. At last, the top Pt layer (20 nm) was deposited by sputtering and lift-off process.

Crack Formation: After completing the device fabrication, the crack-forming process was performed through applying a triangular waveform repeatedly (illustrated in Figure S15, Supporting Information), where voltage step is 1 V and time duration for each step is 1 s. The maximum value of voltage (V_{gmax}) increased progressively with a step of 2 V until the crack is induced. The V_{gmax} used for the device with L_g = 6 μm was 24 V. The crack formation for the device with L_g = 300 and 500 nm was using the ±20 V pulses with a duration of 1 s.

Electrical Measurement: The electrical performance of nanocrack switching was measured through Agilent B1500 or Keithley 2400 and 2450. The electrical performance of logic gates was measured by the combination of Keithley 2410 and 2182A. Note that in the logic gates measurement, the applied signal V_1 (Figure 5f) had voltage levels of ± 20 V and V_2 (V_3) was + 0.5 V (representing for V_{DD}) or 0 V (representing for GND).

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

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Conflict of Interest

The authors declare no conflict of interest.

Author Contributions

Z.G. and Y.G. contributed equally to this work. Z.G. and L.Y. conceived the idea. Z.G. deposited the film. Y.G. and Q.L. fabricated the devices. Z.G. and Y.G. performed the electrical measurements. Y.G. conducted the SEM characterizations. Z.G, Y.G., and L.Y. wrote the manuscript. All authors commented on the manuscript.

Data Availability Statement

Research data are not shared.

Keywords

ferroelectric nanocracks, ferroelectronics, logic-in-memory devices, low power consumption, zero off-current

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