Journal of Magnetism and Magnetic Materials 494 (2020) 165739

Contents lists available at ScienceDirect

Journal of Magnetism and Magnetic Materials

journal homepage: www.elsevier.com/locate/jmmm

Research articles

Skyrmion latch and flip-flop in magnetic nanotracks with gradient anisotropy

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ABSTRACT

Skyrmion sequential elements are proposed and demonstrated. A skyrmion latch is implemented in a single device where skyrmion motion is controlled by spin-orbit torque and voltage-controlled magnetic anisotropy in a magnetic nanotrack with gradient anisotropy. Micromagnetic simulations have been carried out to verify the feasibility of the latch function and to study device performance. The results indicate that the proposed skyrmion latch have potential advantages, including a small device footprint, a tunable switching speed, and low power consumption. Furthermore, a master-slave skyrmion flip-flop can be simply implemented by cascading two skyrmion latches to be further used for constructing a skyrmion register. This work provides a guideline to design spintronics for sequential logic circuits.

Spin logic circuits are potential candidates for the beyond-CMOS computing paradigm, owing to their low power dissipation and data nonvolatility [1–4]. Magnetic skyrmions [5–7], particle-like spin structures with a whirling configuration, are used as the information carrier for constructing skyrmion-based spin logic devices. Thus far, several skyrmion logic gates have been proposed [8–11], in which logic functions are mainly implemented by manipulating skyrmion motion in magnetic nanotracks to transfer the information from input to output ends. However, these existing skyrmion-based logic devices can only serve the combination logic circuit. From the view of practical application, sequential elements, including the latch and the flip-flop, were not addressed. These items are crucial to sequential logic circuits and digital signal processing applications [12].

In this work, skyrmion latch and flip-flop architectures are proposed and studied, in which skyrmion motion is manipulated by various effects, including gradient anisotropy (GA) [13–16], spin orbit torque (SOT) [17–19], and voltage-controlled magnetic anisotropy (VCMA) [20–22]. The enable signal associated with VCMA is used to control the propagation and block of skyrmion motion, implementing the latch function. Performance evaluation results show that skyrmion-based latch and flip-flop have advantages, including high density, tunable switching speed, and low operating power, realized in single structures, which would broaden skyrmion applications (*e.g.*, skyrmion-based registers).

Fig. 1(a) shows a magnetic nanotrack comprised of a heavy metal (HM)/ferromagnetic (FM) bilayer with a skyrmion in the FM layer. The FM layer has a GA. That is, the perpendicular magnetic anisotropy (PMA) constant, K_u, increases linearly along the length of the nanotrack in the x direction as $K_u = K_{u0} + gx$, where K_{u0} is the PMA constant at left boundary, and g is the slope of the GA. This can be effectively realized by manipulating the thickness of the FM layer [23] or the insulator layer (not shown) capping on the FM layer [24–26]. Particularly, GA in the skyrmion device has been experimentally realized by adding an insertion layer with varying thickness between FM and insulator layers [27], or manipulating the film thickness in an antiferromagnet (AFM)/FM material system [28]. GA in a nanotrack can induce the skyrmion into a steady motion in the direction of decreasing anisotropy and energy, as shown in Fig. 1(b). A drive current flowing through the HM layer causes the injection of a spin current into the FM layer to move the skyrmion via SOT. When drive-current density (J_d) is larger than the critical depinning current density (J_c), the skyrmion moves to the right side with a high energy state (Fig. 1(c)). A local voltage (V_g) is used to construct a gate for controlling skyrmion motion via the modification of local anisotropy energy of FM films (*i.e.* VCMA). When V_g is on, K_u increases in the controlled region, resulting in the skyrmion motion being blocked. Thus, the skyrmion maintains its previous position at either the left or right side, as shown in Fig. 1(d). Overall, the skyrmion's position in FM layer can be manipulated by combining the effects described, paving the way for implementing the latch function, as described below.

Skyrmion dynamics in the FM layer are studied using micromagnetic simulation by solving LLG equation with an SOT term using OOMMF [29]. The default simulation parameters, based on commonly used values [17], are listed as follows. The simulation mesh size is $1 \times 1 \times 1\ nm^3$ with one cell in the thickness direction. The exchange constant (A_{ex}), the *Dzyaloshinskii – Moriya* interaction constant (A_{DMI}),

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https://doi.org/10.1016/j.jmmm.2019.165739
Received 23 July 2019; Received in revised form 21 August 2019; Accepted 23 August 2019
Available online 23 August 2019
0304-8853/

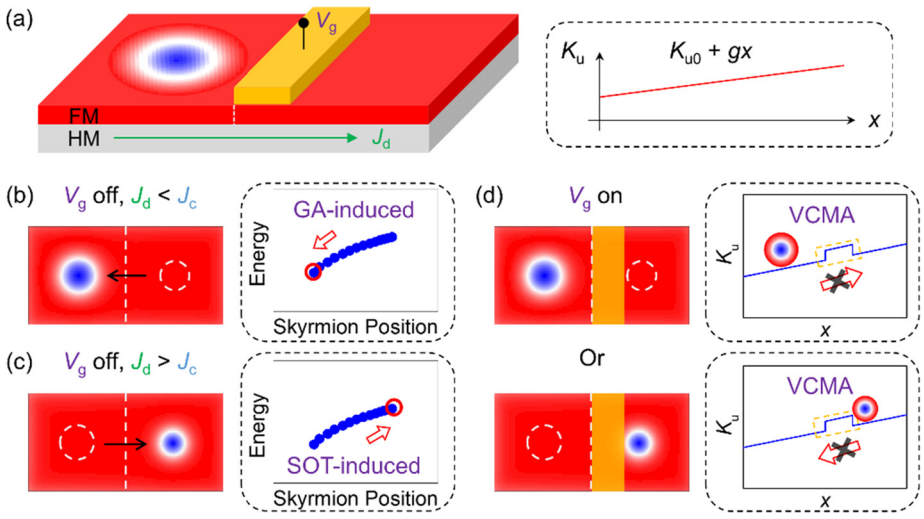

Fig. 1. (a) Schematic of a magnetic nanotrack comprising an HM layer and an FM layer with GA along the length of the nanotrack (x direction). A local voltage (V_g) is used to modify the anisotropy of the FM film. (b,c) Final states and energy profiles along the × direction in FM layer for the cases of (b) V_g off, J_d (drive current density) < J_c (critical current density), and (c) V_g off, J_d > J_c. (d) Final states and PMA constant (K_u) along the × direction in FM layer for the case of V_g on.

the saturation magnetization (M_S), the *Gilbert* damping constant (α), and the spin Hall angle (θ_{SH}) are 15 pJ/m, 3 mJ/m^2, 580 kA/m, 0.3, and 0.4, respectively. Varied J_d and GAs with varied K_{u0} and g are adopted to evaluate the performance of the skyrmion latch. K_u in the voltage-controlled region is assumed to increase to 1.1 times when V_g is on [22].

Based on the above structure, a skyrmion latch is further constructed using two magnetic tunnel junction (MTJ) stacks placed at the left and right sides of the nanotrack. One is the output (Q) and another is its complement ($\bar{Q}$), as shown in Fig. 2(a). Here, the absence of a skyrmion below the Q-end causes a low-resistance state (LRS) of the MTJ at right side, denoted as $Q = 0$, whereas $Q = 1$ corresponds to presence and high-resistance state (HRS). An individual skyrmion moves between Q- and $\bar{Q}$-end, and this feedback thereby ensures Q and $\bar{Q}$ remain in a constant state with $\bar{Q}$ as the complement of Q (*i.e.* the bistable states of the latch). D is the input with two binary states, 0 and 1, to identify J_d less and larger than J_c, respectively. The enable signal (E) determines the V_g off ($E = 0$) and on ($E = 1$). According to the results shown in Fig. 1(b)–(d), the states of the input, the enable signal, and their corresponding outputs are listed in Table 1 (left). One can see that the data propagates from input D to output Q (*i.e.* $Q = D$) when $E = 0$, and the data transmission is blocked when $E = 1$, thus implementing the level-triggered latch function.

The skyrmion latch is implemented based on a single-device structure, which significantly simplifies the design. The planar area of a skyrmion latch is around 2 $W \times W$, as shown in Fig. 2(b), where W is the width of the nanotrack. The device can be scaled down with the skyrmion size and the stacked MTJ. The skyrmion diameter is around 15–20 nm at $W = 60$ nm, $K_{u0} = 0.6$ MJ/m^3, and $g = 2$ TJ/m^4, and can be sub-10 nm theoretically [17], while the MTJ dimension demonstrated so far is around 40 nm and smaller one is being developed. Thus, W is expected to be at least 40 nm and potentially to be further scaled down. Moreover, the device number of a skyrmion latch is far less than that of the CMOS counterpart, which is constructed from several logic gates and many transistors. With increasing device integration, the greatly reduced device counts are expected to be beneficial for reducing chip footprint. This results from the benefit of fabricating within back-end-of-line technology layers, leaving the extra potential for 3-dimensional monolithic integration schemes. For example, the layout area of a CMOS D latch is more than several hundred F^2 (F is the feature size). In

Table 1
Function table of skyrmion latch and skyrmion flip-flop.

Skyrmion Latch					Skyrmion Flip-Flop				
E	D	Q	$\bar{Q}$	Operation	CP	D	Q	$\bar{Q}$	Operation
0	0	0	1	Reset	↑	0	0	1	Reset
0	1	1	0	Set	↑	1	1	0	Set
1	×	Q	$\bar{Q}$	No Change	×	×	Q	$\bar{Q}$	No Change

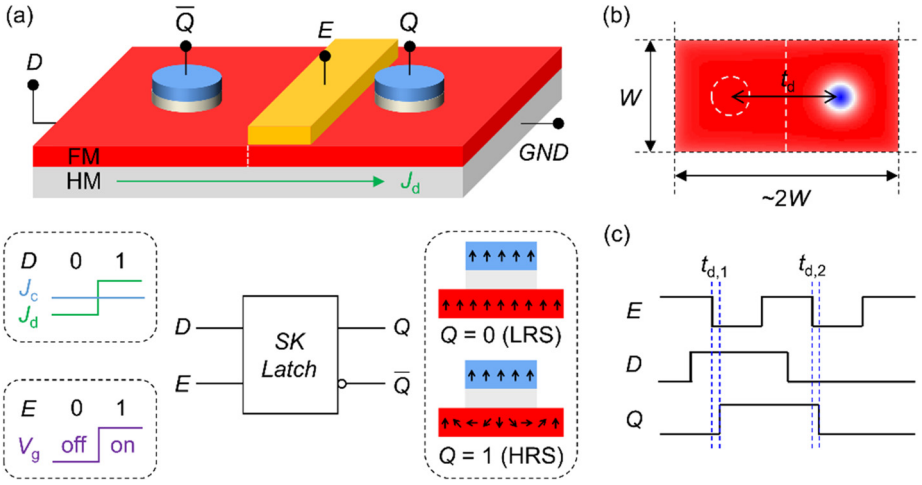

Fig. 2. (a) Schematic of a skyrmion latch with an input (D), two outputs (Q and $\bar{Q}$), and an enable signal (E). (b) Top view of the FM layer with planar area of 2 $W \times W$. (c) Timing sequence diagram of the skyrmion latch.

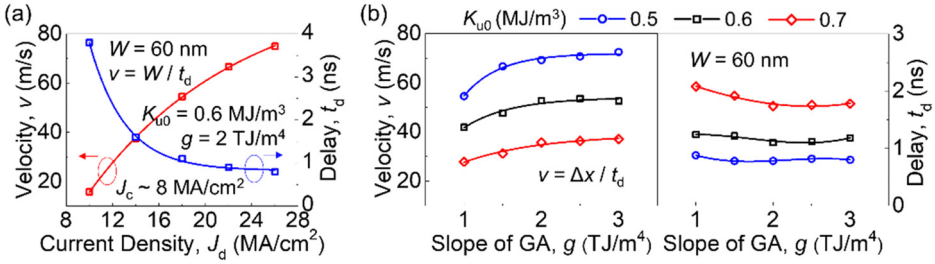

Fig. 3. (a) Velocity (v) and delay time (t_d) of SOT-induced skyrmion motion as a function of drive current density (J_d). (b) v and t_d of GA-induced skyrmion motion as a function of slope of GA (g) under different K_{u0}. K_{u0} is the PMA constant at left boundary of the magnetic nanotrack.

contrast, a skyrmion latch with 40 × 80 nm^2 size is equivalent to only 32F^2 at F = 10 nm. Even accounting for some transistors connected to the input and output ports, the layout area is expected to be smaller than the CMOS counterpart. Therefore, the skyrmion latch is promising for the high-density integrated circuit.

For high-speed register applications, propagation delay time of the sequential elements is a critical performance metric. In the proposed skyrmion latch, two kinds of delay times occur at the moment the output changes with the input (Fig. 2(c)). This results from the SOT- and GA-induced skyrmion motion between Q and $\bar{Q}$. The average velocity (v) of the SOT-induced skyrmion motion and corresponding propagation delay time (t_d) are shown in Fig. 3(a), where t_d is obtained from simulations, and v is approximately calculated by $v = W/t_d$. The devices with W = 60 nm are investigated. When material parameters are given, v increases with J_d at $J_d > J_c$ (here, $J_c \sim 8$ MA/cm^2). Note that maximum velocity (v_{max}) is limited by the skyrmion Hall effect (SkHE) [30,31]. When J_d is sufficiently large (here, > 28 MA/cm^2), the skyrmion touches the boundary of the nanotrack and is destroyed. In our case, v_{max} is around 80 m/s at $J_d \sim 26$ MA/cm^2, and the corresponding t_d is sub-ns (0.8 ns). If methods are adopted to suppress the SkHE [32,33] and increase the skyrmion velocity to hundreds or even thousands, t_d can be further reduced to 10^1–10^2 ps scale.

Regarding GA-induced motion, v and t_d depend on the GA properties, including K_{u0} and g, as shown in Fig. 3(b). Note that the skyrmion size in the nanotrack is also changed with K_u. Hence, the motion distance (Δx, not shown) is slightly different under different cases of the GA, and here, v is approximately calculated by $v = \Delta x/t_d$. The results suggest that t_d can be simply tuned by changing K_{u0}. At K_{u0} = 0.5 MJ/m^3, t_d is at the sub-ns scale. Additionally, there is a working window of K_u for skyrmion stability when the other material parameters are given. In this work, the skyrmion would be annihilated at a region with K_u > 1 MJ/m^3.

Overall, the propagation delay time of the skyrmion latch can be effectively improved by tuning v by properly increasing J_d and decreasing K_{u0}. Besides, decreasing W (*i.e.* scaling down the device) can also reduce t_d because of the reduced Δx. On the other hand, the circuit simulation has shown that the delay time of the skyrmion detection by output MTJ is tiny (~25 ps) [9].

The static power of the skyrmion latch is related to the enable operation at E = 1 (V_g on) to retain the latch state. This enable operation, based on VCMA, is energy efficient, because the voltage is applied on an insulator layer, leading to extremely low static power consumption. Therefore, the power consumption is dominated by SOT-driven skyrmion motion. This dynamic power (P_d) is mainly caused by *Joule* heat generated by drive current, and can be estimated as

$$P_d = I_d^2 R t_p = (J_d \cdot W \cdot H)^2 \cdot [\rho \cdot L/(W \cdot H)] \cdot t_p = J_d^2 \cdot \rho \cdot W \cdot H \cdot L \cdot t_p = J_d^2 \cdot \rho \cdot V \cdot t_p \quad (1)$$

where, I_d is the drive-current amplitude, t_p is the current pulse width, and R, ρ, W, H, L, V are the resistance, resistivity, width, thickness, length of HM layer, respectively. Here, we assume the HM layer with ρ ~ 190 μΩ·cm and V = 120 (L) × 60 (W) × 5 (H) nm^3. If a drive current of J_d = 20 MA/cm^2 and t_p = 1 ns is applied for the case of D = 1, it corresponds to a low energy consumption of ~3 fJ per operation. If the high-θ_{SH} materials (*e.g.*, topological insulator with $\theta_{SH} \sim 52$ [34]) are to be used, J_d can be substantially reduced for lower power consumption. Besides, the power dissipated in the output MTJ during the sensing period is also of the order of a few fJ [9].

A master–slave skyrmion D flip-flop (DFF) is further realized by cascading skyrmion latches. In this scheme, the stored data of a skyrmion latch is encoded by magneto-resistance, not the voltage signal like in CMOS counterparts. Thus, a read current (J_r) is needed through the output MTJ of the prior latch (*i.e.* master latch) to obtain the output voltage (V_{out}), as shown in Fig. 4(a). V_{out} is then transferred to the input D' of the post latch (slave latch), and its strength determines whether J_d is larger than J_c in the slave latch, realizing the cascading. The function table and timing-sequence diagram of the skyrmion DFF are shown in Table 1 (right) and Fig. 4(b), respectively. At CP = 0 ($\bar{CP}$ = 1), the master skyrmion latch is transparent, whereas the slave latch is opaque. With the advent of the CP rising edge, accompanied by the current pulse J_r, the slave latch becomes transparent and gets the stored data of the master latch to transmit it to the output, thus implementing the rising-edge-triggered DFF function. Using several skyrmion flip-flops, a skyrmion-based register can be further constructed. A 4-bit shift register design formed with DFF cells is shown in Fig. 4(c).

In summary, skyrmion latches and flip-flops are implemented by manipulating skyrmion motion via SOT and VCMA in magnetic nanotracks with GA. Physics-based simulations indicate that the proposed

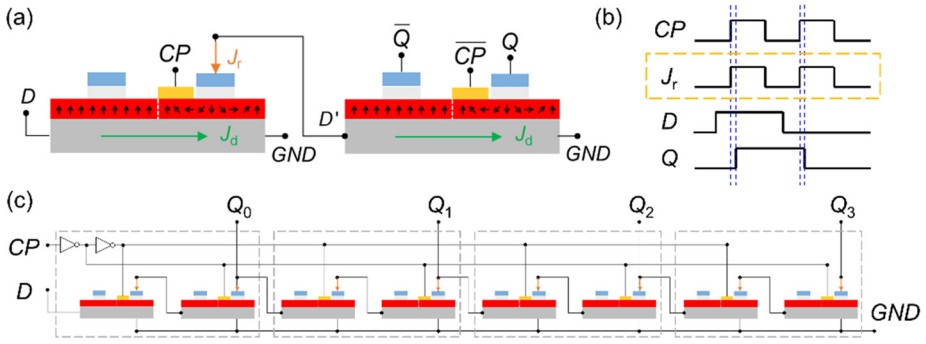

Fig. 4. (a) Schematic of a skyrmion flip-flop via two cascaded skyrmion latches. A read current (J_r) is needed applying through the output MTJ of the prior latch to obtain the output signal, which is transferred to the input D' of the post latch. (b) Timing sequence diagram of the skyrmion flip-flop. (c) Schematic of a 4-bit shift register design formed with skyrmion flip-flops.

skyrmion latch has potential advantages, including a small device footprint, a tunable switching speed, and low power consumption. A skyrmion flip-flop is constructed by connecting the master and slave skyrmion latches and is further used to build the skyrmion register. These skyrmion-based sequential elements have the promising potential to provide spin-based sequential logic circuits.

Acknowledgments

This work was supported by the National Natural Science Foundation of China [Grant Nos. 61674062 and 61821003] and the Fundamental Research Funds for the Central Universities, HUST: 2019JYCXJJ010.

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